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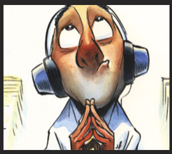

HOP, JUMP, AND SPREAD: WIRELESS MACHINE-TO-MACHINE INTERFACES

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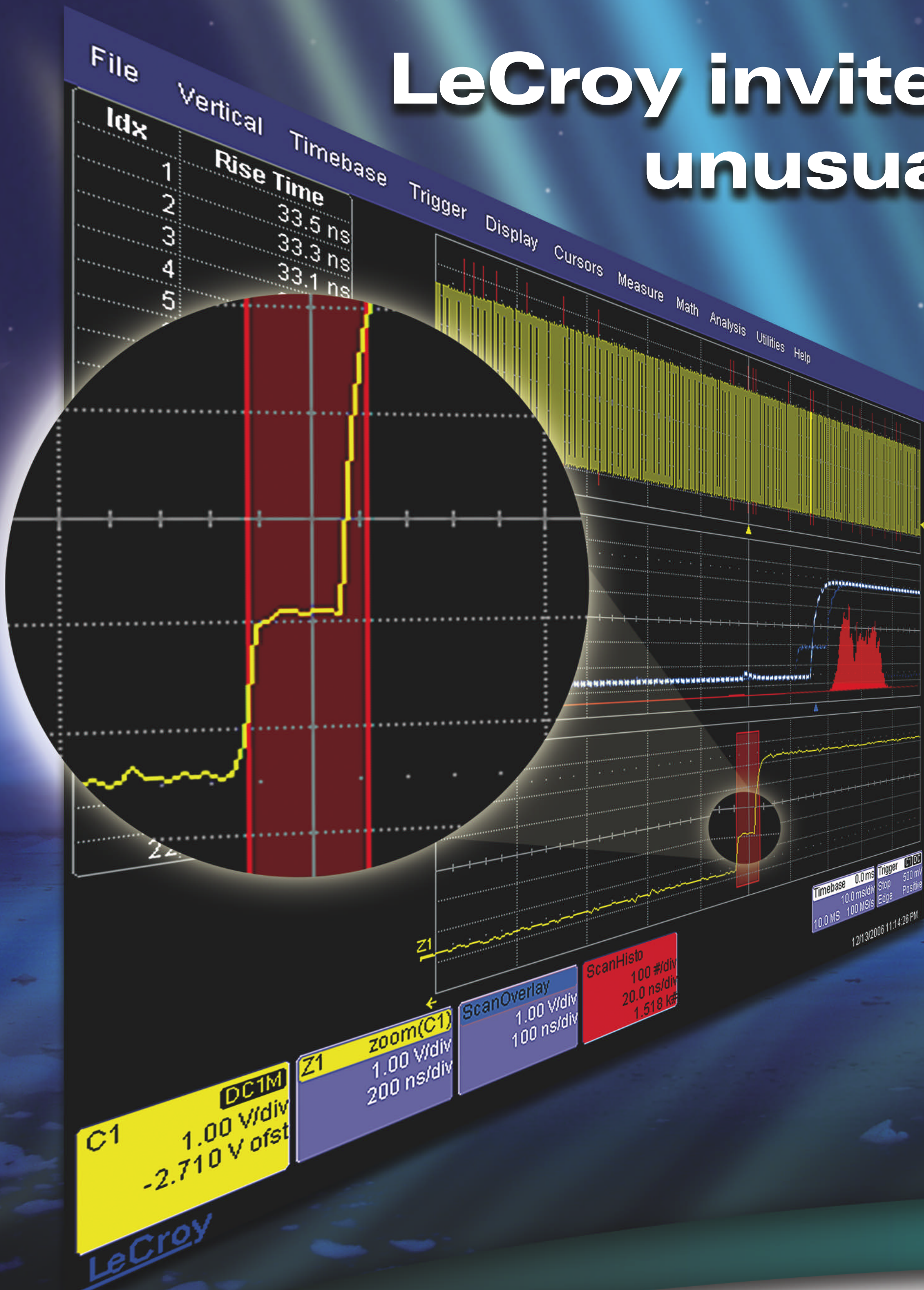
LeCroy invites you to unusual events.



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EDN Magazine has included LeCroy's WaveRunner® Xi and WaveSurfer® Xs with WaveScan in it's 'Hot 100 Products' list. WaveScan is also an EDN 2007 Innovation Award Finalist.

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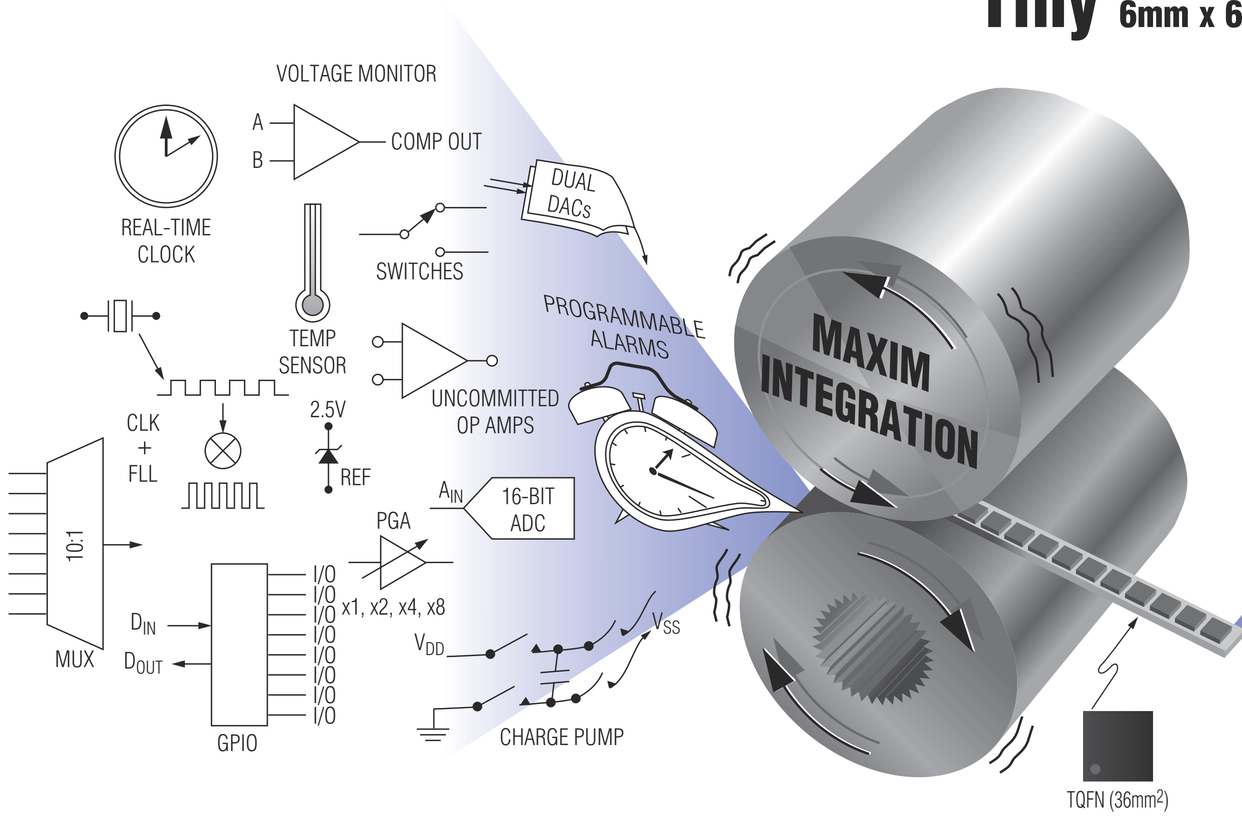

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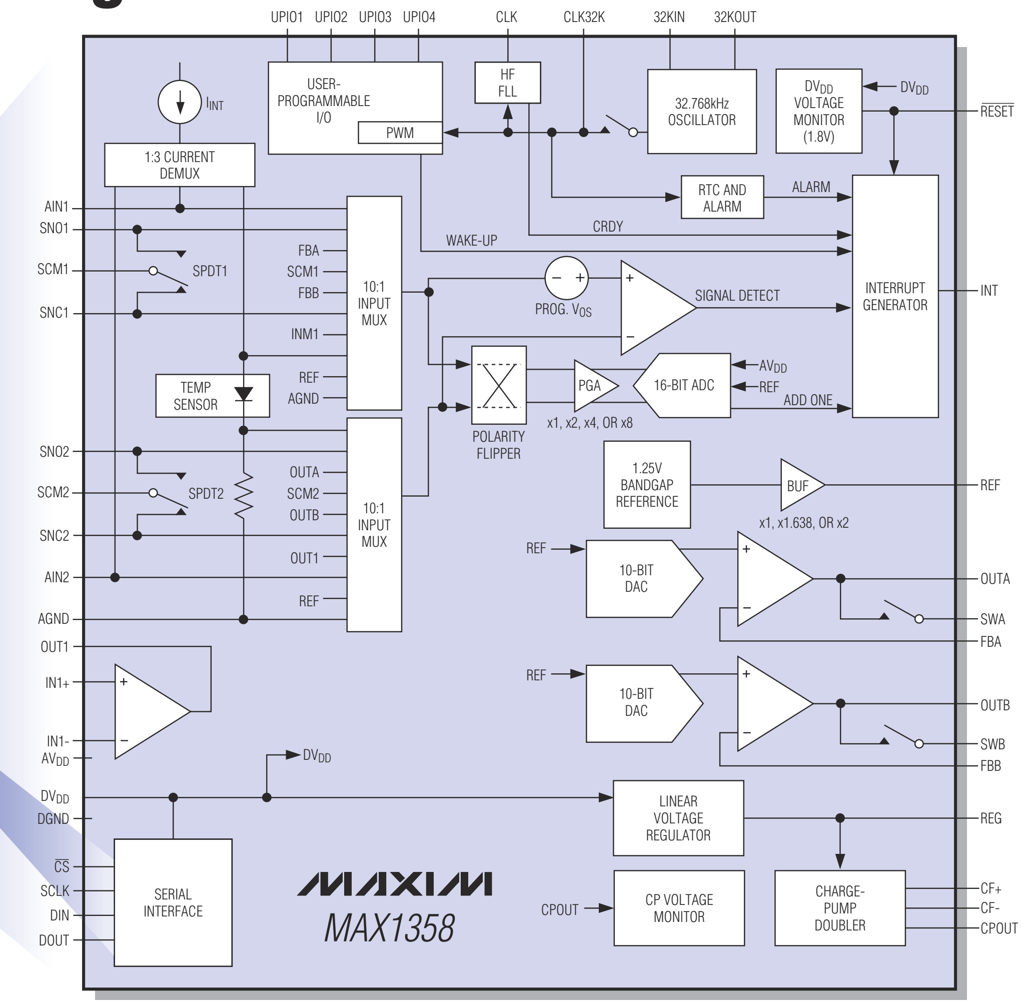

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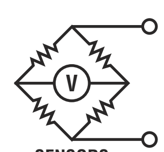
MAX1358	16-bit, sigma delta	2	0.01 to 0.512	2 x 10-bit F/S**	1	4	2/2	8.07
MAX1359	16-bit, sigma delta	2	0.01 to 0.512	1 x 10-bit F/S**	2	4	2/1	7.45
MAX1360*	16-bit, sigma delta	2	0.01 to 0.512	0	3	4	2/0	*

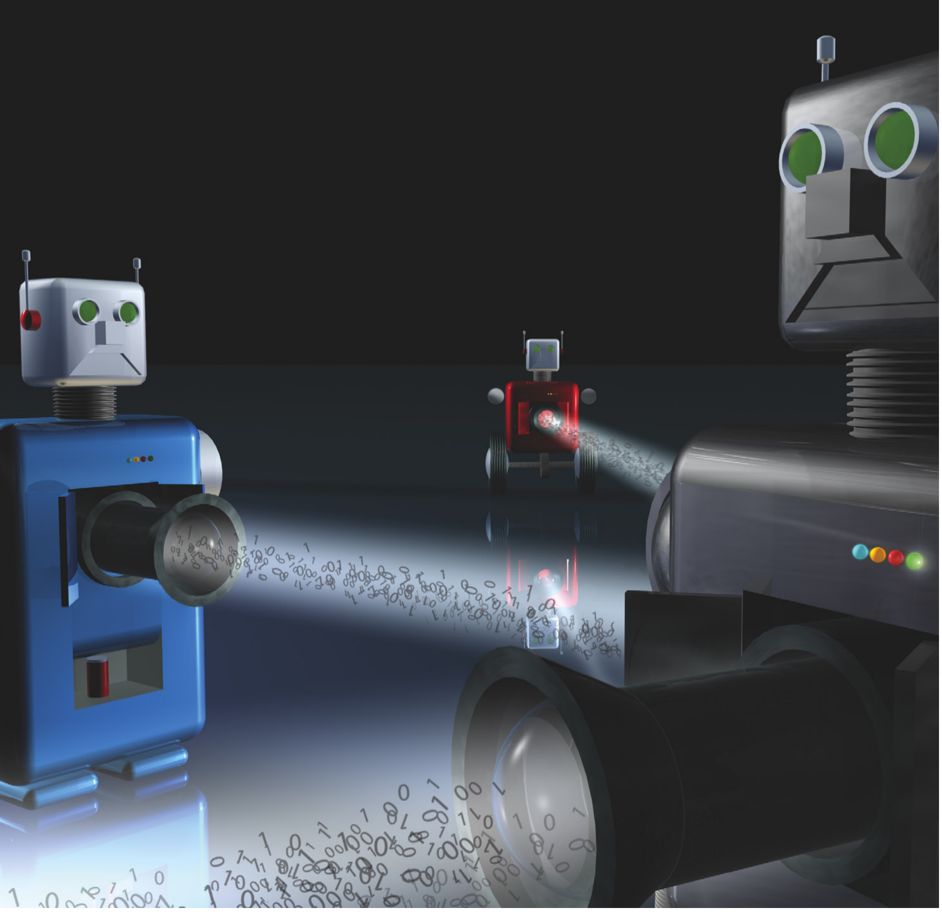
PORTABLE MEDICAL DEVICES

MEDICAL INSTRUMENTS



SENSORS

*Future product—contact factory for availability.
** F/S = Force-sense.
†1000 piece price provided is for design guidance and is FOB USA. International prices will differ due to local duties, taxes, and exchange rates Not all packages are offered in 1k increments, and some may require minimum order quantities.



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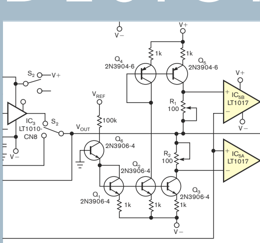

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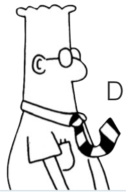

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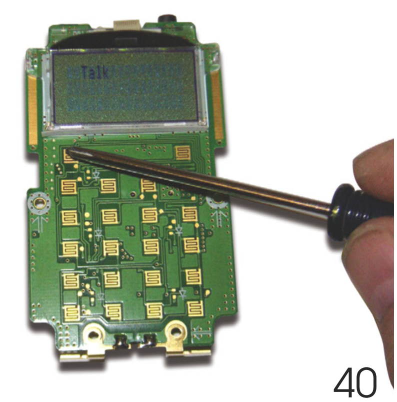

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DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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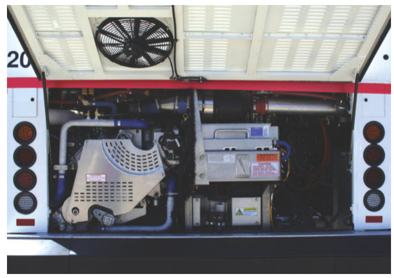

READERS' CHOICE

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Microcontroller functions as voltmeter
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VIDEO DESIGN IDEAS

Visit *EDN*'s Tech Clips page to view Design Ideas in video format. The premiere Video Design Idea features Jim Williams, staff scientist at Linear Technology, explaining why PC clocks are invariably wrong and how engineers can surmount the extreme measurement challenge involved in solving the problem.
→www.edn.com/techclips

READY FOR REACH?

Not long after the hassle of complying with ROHS, a new challenge comes into play this month: the European Union's REACH (Registration, Evaluation, and Authorization of Chemicals) regulation. REACH controls the use of thousands of chemicals, many of which find use in the electronics supply chain. To learn more about the regulation and how it will affect your electronics supply chain, see our *EDN* guide to REACH.
→www.edn.com/guides/reach.html

2007 *EDN* DSP DIRECTORY

A comprehensive listing of digital-signal-processing resources, including software-programmable processors, programmable fabrics, IP (intellectual-property) blocks, and digital-signal controllers.
→www.edn.com/dspdirectory

BY MAURY WRIGHT, EDITORIAL DIRECTOR

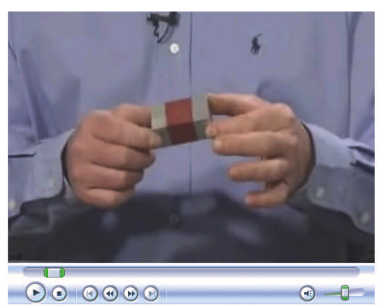
Internet video provides another channel for Design Idea delivery

If you've recently visited EDN.com, I hope you've noticed a number of enhancements. We've begun to offer short tutorial and how-to video programs, including video versions of our always-popular Design Ideas. And, as we detailed in an earlier column, we've redesigned the Web site using a community structure to make it easier to use (**Reference 1**). We've also just launched Part Search—a real-time pricing and inventory tool. I'd certainly like you to give EDN.com a spin and tell me what you think. I'd also invite you to participate.

I'm not a big fan of the term "Web 2.0." It's a bit absurd to think of new Web developments happening in discrete chunks. But without a doubt, full-duplex communication is becoming prevalent on the Web. We've long welcomed reader comments in the Feedback Loop associated with each article. And our blogs receive quite a few animated comments. With our redesign and our new video capabilities, we've opened the doors to more two-way information flow.

EDN has always depended on readers to write deeply technical contributed articles with a how-to slant and to provide the shorter Design Ideas that are universally popular. So, of course, we want you to participate in the video movement. Go to www.edn.com/techclips to view both our Video Design Ideas and some signal-integrity tutorials from columnist Howard Johnson. Then, think about what *you* might contribute.

We're still working through the logistics of video contributions. We started with reader research. In a recent technology-usage study among our readership, almost 80% of the respondents had viewed Web-based videos. The respondents were interested in how-to-design videos. But it's clear that time is a precious commodity. Indeed, 38% prefer video programs lasting three to five minutes, although 31% indicate a preference for videos of six to 10 minutes. We've decided to target five minutes for our video presentations. So, we are looking for finely focused topics that allow the presenter to quickly make the pertinent points. As we've done with the first Video Design Ideas, we'll try to augment the presentation with information such as schematics available as PDFs.



If you have videography skills and want to submit a finished video, contact me or EDN.com Editor in Chief Matthew Miller directly. If you have a great idea but no way to capture the footage, call me anyway, and we can discuss it. For the moment, we have no automatic way for readers to upload videos, but that capability is coming soon.

Of course, videos are just the newest opportunity for you to participate in the *EDN* community. With the redesign of our Web site at the beginning of April, we opened our doors for you to submit reference designs. We're also allowing the marketing community to directly post new-product releases to augment our own new-product coverage.

Our goal with video and other multimedia presentations is to provide you information in whichever ways you want to consume it. We remain committed to our print product. For print, we still need contributed articles, Design Ideas, and Tales from the Cube. We'll do our best to optimally use the combination of print, Web, and e-mail channels. Based on the response to our early work with videos, it's clear that some of you really like that option for receiving information.

Finally, please try Part Search (www.edn.com/partsearch). Enter the part number of an IC, and you'll get the current price and delivery information. You can view recent price trends and even get a data sheet. **EDN**

REFERENCE

1 Miller, Matthew, "10 reasons to visit EDN.com," *EDN*, April 26, 2007, pg 12, www.edn.com/article/CA6434364.

Contact me at mgwright@edn.com.

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Frequency Range	290-980	MHz
Voltage Supply	2.2-3.6	V
Temperature Range	-40 to +125	˚C
Output Power	10	dBm
I_{TOT}	18	mA
I_{PD}	<1	µA

For more information, contact your local Micrel sales representative or visit us at www.micrel.com/ad/micrf405.
Literature: 1 (408) 435-2452
Information: 1 (408) 944-0800

Applications:

- Remote control systems
- Residential automation
- Wireless security system
- Meter reading
- Automotive
- Smart home

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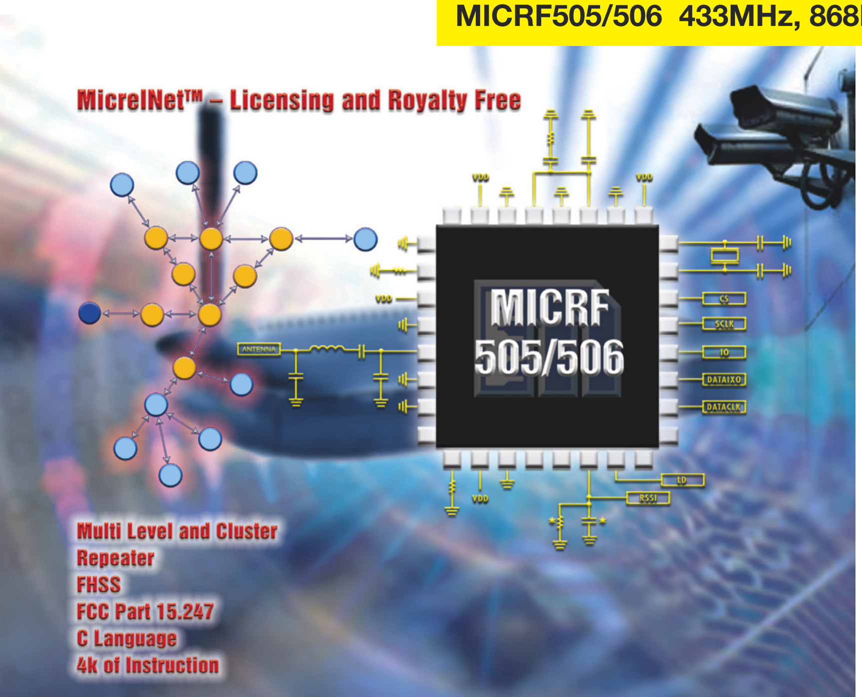
MICRF505/506 433MHz, 868MHz and 915MHz ISM Band Transceiver



The new MICRF505/506 are true single-chip frequency shift keying (FSK) transceiver devices intended for use in half-duplex, bidirectional RF links. The multi-channel FSK transceiver is intended for UHF radio equipment in compliance with the North American FCC, as well as European ETSI.

	MICRF505	MICRF506	Unit
Frequency Range	850-950	410-450	MHz
Data Range	<200	<200	kbps
Sensitivity	–112	–113	dBm
Output Power	10	11	dBm
Tx Current	28	21	mA
Rx Current	13	12	mA

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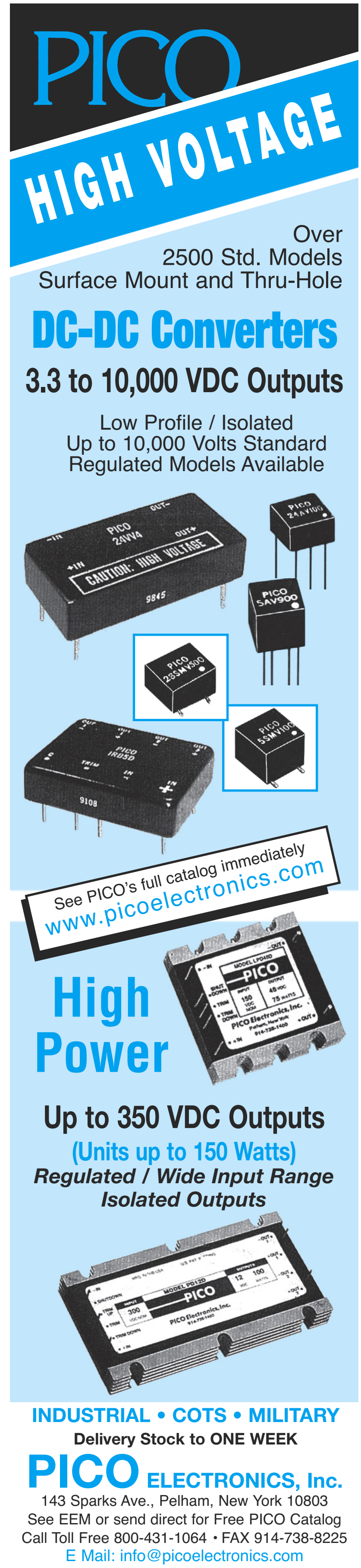
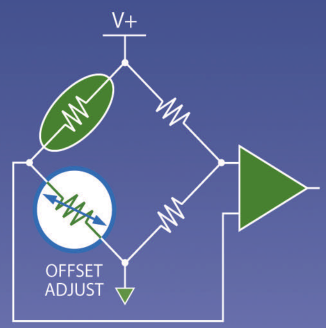
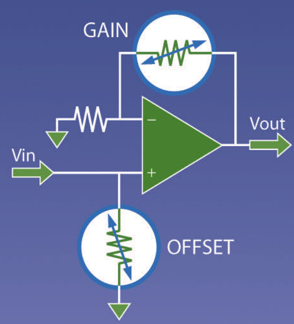


Do you use Rejustors?

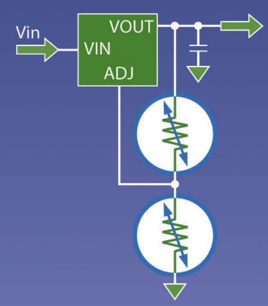
If your design needs precise calibration and/or compensation then look at the details that follow. As the name suggests, Rejustors are re-adjustable resistors. This easy, automated, cost-effective approach to calibration/compensation eliminates hand selection, analog and digital potentiometers and thick/thin film resistor laser trimming. Microbridge holds multiple patents on Rejustor™ technology and leads the industry in developing new applications and licensing of Rejustors for on-chip integration.



Sensor Compensation



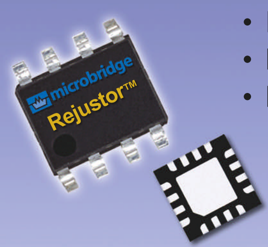
Amplifier Calibration



Voltage Regulator Adjustment

Features

- Passive, non-volatile variable dual resistor, requires no power
- Resolution to 0.01%
- Bidirectional adjustment
- Absolute TCR 0±100ppm/K
- Relative TCR 0±10-50ppm/K



Benefits

- Single chip solution for precision adjustment of voltages, currents, offsets, gains, and more
- Improved reliability, dust and moisture resistant
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- Flexibility reduces rework cost

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Low Power Product - Available in QFN

Part Number	Ratio	Resistance Range R1	Resistance Range R2
MBD-472-AL	1:1	3.3K - 4.7K	3.3K - 4.7K
MBD-902-AL	1:1	6.3K - 9K	6.3K - 9K
MBD-153-AL	1:1	10.5K - 15K	10.5K - 15K
MBD-333-AL	1:1	23K - 33K	23K - 33K
MBD-153-KL	1:3	10.5K - 15K	31.5K - 45K
MBD-472-CL	1:5	3.3K - 4.7K	16.5K - 23.5K
MBD-902-CL	1:5	6.3K - 9K	31.5K - 45K
MBD-103-XL	1:7	7K - 10K	49K - 70K

Standard Product - Available in QFN or SOIC

Part Number	Ratio	Resistance Range R1	Resistance Range R2
MBD-153-AS	1:1	10.5K - 15K	10.5K - 15K
MBD-472-AS	1:1	3.3K - 4.7K	3.3K - 4.7K
MBD-903-AS	1:1	63K - 90K	63K - 90K
MBD-103-AS	1:1	7K - 10K	7K - 10K
MBD-103-BS	1:2	7K - 10K	14K - 20K
MBD-103-CS	1:5	7K - 10K	35K - 50K
MBD-103-ES	1:9	7K - 10K	63K - 90K

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POWER designer

Expert tips, tricks, and techniques for powerful designs

No. 118

Saving Energy via Smart Power Management

— By Michael Drake, Applications Engineer

Power management techniques and methodologies are expanding rapidly. Political, environmental, and consumer-driven pressures are pushing the market toward increasing functionality while decreasing power consumption. Portable applications, in particular, are presently seeing a great deal of expansion. It is a growing market segment that is being fueled by the increase of wireless devices and their expanding feature sets. Cellular telephones, PDAs, MP3 players, digital cameras, and portable gaming platforms are getting smaller, faster, and more capable. In order to maintain acceptable levels of "talk-time" (battery life), a great deal of effort is being put into the design of the power-supply subsystems.

Power conversion and system energy management are two primary areas that affect battery life in portable equipment. Power conversion deals with the efficient transformation of the battery voltage into the required supply rail(s), while system energy management attempts to conserve energy by optimizing the entire system to the real-time needs of the application.

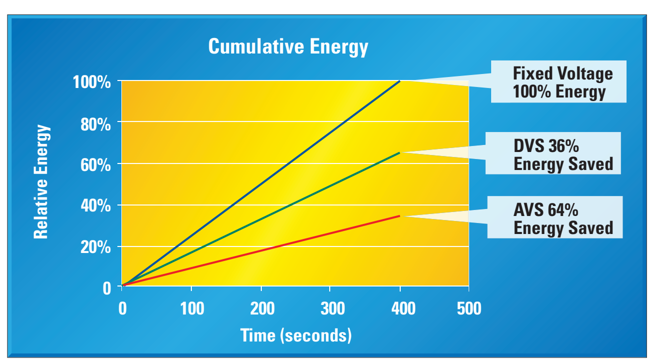


Figure 1. Energy Savings with DVS and AVS

Optimizing Regulation Yields Energy Solutions

The power conversion challenge is to maximize the efficiency of the regulators. The efficiency of a regulator is defined as the output power over the input

NEXT ISSUE:

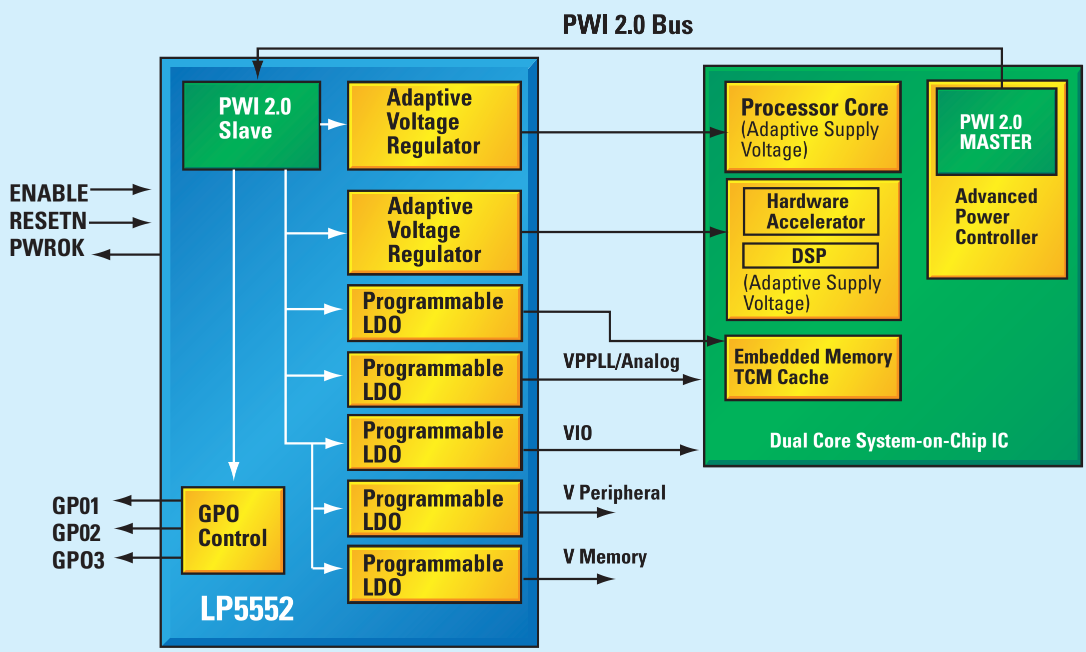
Lighting for Handhelds

National Semiconductor

The Sight & Sound of Information

Reduce Energy Consumption with PowerWise® Technology

Digitally-Programmable LP5552 Energy Management Unit Extends Battery Life and Enables New Features



AVAILABLE LEAD-FREE

Product ID	# of Outputs	Output Voltages and Current	V_{IN} Range	Interface	Package
LP5550	4	1 Buck: 0.6V to 1.2V, 300 mA 3 LDOs: 0.6V to 3.3V, up to 250 mA	3V to 5.5V	PWI 1.0	LLP-16
LP5551	8	2 Bucks: 0.6V to 1.2V, 300 mA 4 LDOs: 0.6V to 3.3V, up to 250 mA N-well bias: -0.3 to +1V (to supply) P-well bias: -1V to +0.3V (to GND)	2.7V to 5.5V	PWI 1.0	LLP-36
NEW **LP5552**	7	2 Bucks: 0.6V to 1.235V, 800 mA 5 LDOs: 0.6V to 3.3V, up to 250 mA	2.7V to 4.8V	PWI 2.0	micro SMD-36

Ideal for use in dual core processors, cellular handsets, handheld radios, PDAs, battery-powered devices, and portable instruments

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Saving Energy via Smart Power Management

power and is given as a percentage:

$$\eta = P_{OUT} / P_{IN} = (V_{OUT} * I_{OUT}) / (V_{IN} * I_{IN})$$

Power conversion efficiencies now reach into the 90th percentile and increases are becoming more difficult to realize. As conversion efficiency has reached a plateau, it has become necessary to find new ways to conserve energy at the system level. This gets into the realm of energy management.

The following two equations show the necessity for system energy management. There is the dynamic term involving C, the circuit capacitance, the supply voltage, V_{DD}, and *f*, the clock frequency. The second term is the static term which is dominated by the leakage current of the digital gates. In larger-geometry devices, the dynamic term dominates the power utilization. As the industry moves to ever-smaller devices, the static term is becoming increasingly important.

In a digital system, the power consumed is roughly equal to:

$$P = (C * V_{DD}^2 * f) + (V_{DD} * I_{LEAK})$$

Thus, the energy expended is roughly equal to:

$$E = (C * V_{DD}^2) + ((V_{DD} * I_{LEAK}) * t)$$

Several Techniques Exist for Design Improvements

Almost all large digital systems will deploy one or more clock-gating strategies to avoid unnecessary toggling of the clock, and many systems will power-down unused sections of the design when appropriate. Processing engines also make use of idle and sleep modes to save energy. This is a conventional energy management technique whereby the processor wakes up periodically, or when required, performs its pending tasks, and then returns to a low-power state. These techniques can be effective, but come at a cost. Any time the circuitry is needed, there is some delay while it is powered up and/or synchronized. These methods conserve energy only when there is nothing to do (i.e., when the processor is in the sleep state).

Newer techniques have involved scaling the frequency and voltage of the processing engine to reduce energy expenditure. Energy is the key metric for increasing ON-time in dealing with battery-powered systems. Dropping the frequency alone will reduce the average power consumption, but it will not reduce the total energy used to complete a specific computational task. The voltage in the system must be reduced to realize energy savings. Dynamic Voltage Scaling (DVS) and Adaptive Voltage Scaling (AVS) both can achieve a reduction in voltage, refer to Energy Savings with DVS and AVS in ***Figure 1***.

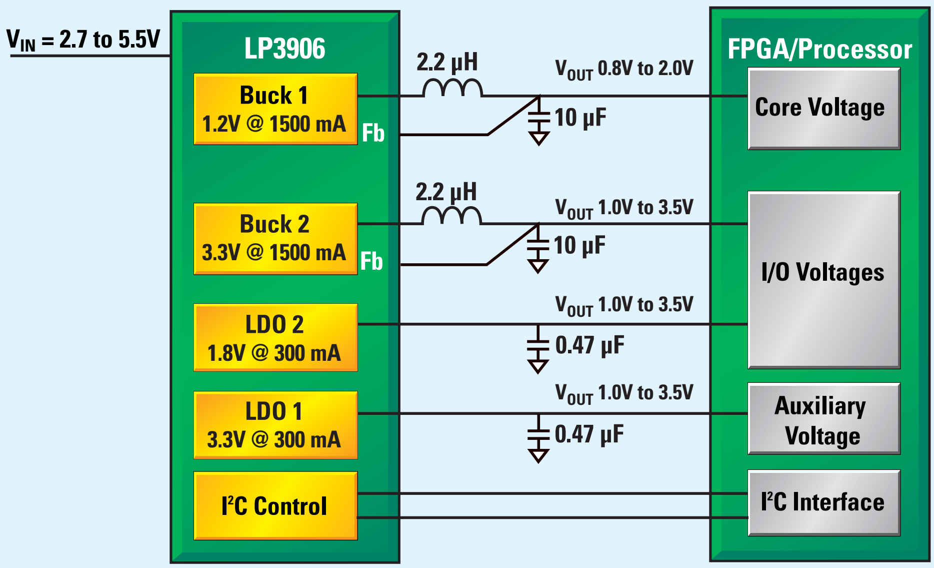
DVS adjusts the voltage and frequency in pre-characterized pairings. National Semiconductor offers Power Management ICs (PMICs) such as the LP3906 and LP3907 devices which support DVS mode as well as devices which support both AVS and DVS modes such as the LP5550, LP5551, and LP5552. DVS provides power and energy savings, with some additional margin in the voltage to accommodate all potential systems over process and temperature variations. This extra overhead to accommodate the worst case results in wasted energy in non-ideal systems. If it was possible to close the power-supply loop at the system level, the control loop could adaptively scale the voltage to the minimum workable voltage and conserve the most energy. PowerWise® technology accomplishes that.

The PowerWise Interface (PWI®) Enables Smart Energy Management

The PowerWise specification is a system-level approach to energy management that enables Adaptive Voltage Scaling (AVS) and state control for battery-powered devices. The PowerWise concept incorporates closed-loop AVS with a high-speed, serial-power-management bus to allow a processing engine to use the minimum voltage at any operating frequency, at any given time in the system, to minimize dynamic energy dissipation.

Easy-to-Use Power Management Units for Digital Subsystems

96% Efficient LP3906 Provides Flexibility with Digital Programmability



LP3906 Features

- Two programmable buck regulators to support core and other high-current rails
- Two programmable LDOs to support internal processor functions and peripherals
- I²C for independent control of LP3906 and peripherals

Ideal for powering application processors, FPGAs, and DSPs where size and efficiency are important

AVAILABLE LEAD-FREE

Product ID	Digitally Programmable	Efficiency	Regulator Output Current	LDO Output Current	Packaging	Solution Size
LP3906	I²C	Up to 96%	1.5 A	300 mA	LLP-24	20 mm x 20 mm
LP3905	N/A	Up to 90%	600 mA	150 mA (low noise)	LLP-14	15 mm x 10 mm

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Saving Energy via Smart Power Management

PowerWise technology also incorporates the ability to bias the well voltages of a processing engine. As V_{DD} is reduced to minimize dynamic losses, the threshold voltage of the transistors must also be reduced to maintain high drive levels. This increases the leakage current and static-power losses. The leakage current can be reduced by back-biasing the well. Alternatively, by forward-biasing it, higher drive levels can be achieved for the same V_{DD}. The PowerWise loop and well-biasing schemes may be used in conjunction with multi-V_T designs.

The standard system configuration to enable PowerWise closed-loop AVS is comprised of an Advanced Power Controller (APC) residing in the processing engine, a PMIC containing a PWI slave, and the 2-wire PWI serial bus connecting the two components. The PMIC supplies various voltages to the processor. The voltage levels provided by the PMIC can be adjusted by sending commands from the PWI master within the APC to the PWI slave.

The APC's task is to accept commands from the host processor, provide a CPU-independent voltage-control mechanism, and track the logic operating speed in real time. The APC is always active and continuously monitors the system over all parameters. System temperature, load, transient, and process variation, amongst others, are all accounted for. As the APC is informed of a pending frequency change, it determines the minimum voltage possible for stable system operation at the new frequency. This occurs within the closed loop to servo the voltage to the appropriate level by using voltage-adjustment commands issued by the APC to the PWI slave via the PWI interface.

Options for Meeting Power Challenges

The PowerWise AVS technology is available with two APC versions. APC1 is for simple single-voltage domain designs and APC2 is suited for more complex multi-domain systems. APC1 uses the point-to-point PWI 1.0 interface while APC2 utilizes the PWI 2.0 bus interface between the master(s) and slave(s).

National offers two Energy Management Units for APC1: the LP5550 device, which includes one AVS DC-DC switcher and three LDOs, and the LP5551 device which adds another DVS-style DC-DC switcher, an additional LDO, and bias regulators for N- and P-well connections in threshold-scaling applications.

The LP5552 Energy Management Unit is compatible with the APC2/PWI 2.0 IP package. The LP5552 device contains two high-performance switching regulators for AVS or DVS applications and five LDOs. All seven regulators are contained in the tiny 36-bump micro SMD package. Each regulator can be independently turned on and off as well as programmed to a desired voltage.

Higher Switching Frequency Enables Reduced Power and Circuit Size

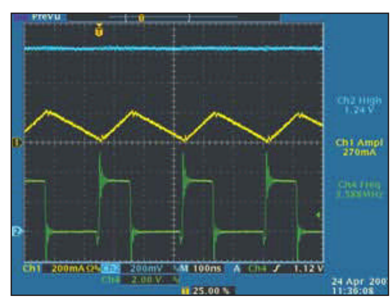
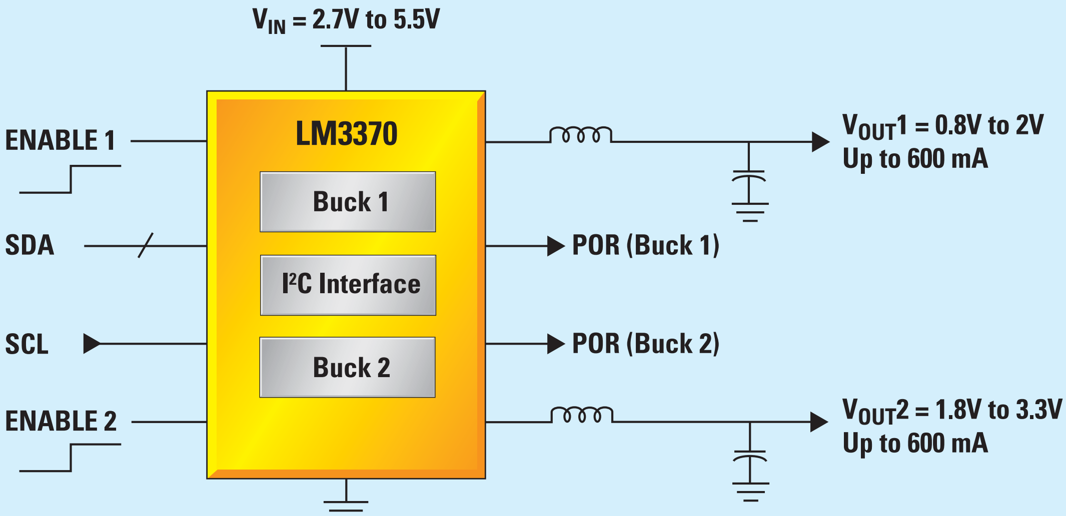


Figure 2. Switcher Output at V_{IN} = 3.6V, V_{OUT} = 1.235V, I_{LOAD} = 400 mA Load

The switching regulators in the LP5552 device operate at a switching frequency of 3.6 MHz as seen in ***Figure 2***. The increased switching frequency allows the use of smaller-valued components for the output filter. Typical values are a 1 µH inductor and a 10 µF ceramic capacitor. These smaller values allow the system designer to select smaller footprint parts with low vertical heights, while maintaining outstanding transient performance.

Enhance Digital Processor Power Management with Dynamic Voltage Scaling (DVS)

LM3370 Dual Buck Regulator Provides Highest Efficiency for FPGAs and Multimedia Processors

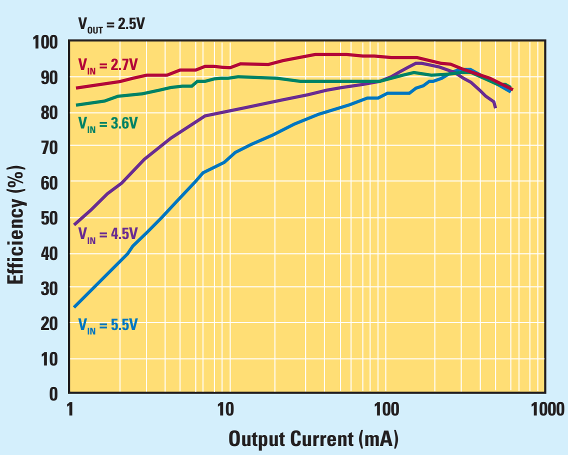


LM3370 Features

- Automatic PFM-PWM mode switching provides high efficiency at all loads
- I²C-compatible interface scales power to match processor clock frequency
- Lowest Iq (<20 µA) extends battery life
- 2 MHz operation enables smaller external components and minimizes footprint
- Power-on-reset prevents fault condition in processors
- Spread spectrum reduces noise (ideal for RF systems)

Ideal for low-power FPGAs, CPLDs, and application processors

High Efficiency Across All Loads



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Saving Energy via Smart Power Management

Transient performance of the switchers can be seen in *Figure 3*. The entire power system can be realized in a sub-0.85 mm height allowing extremely thin form factors in the product design.

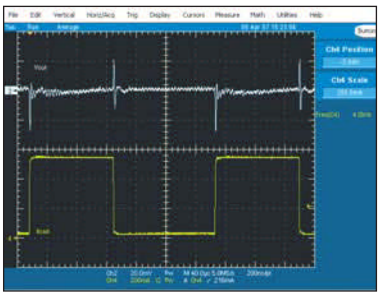

Figure 3. 50 mA to 560 mA to 50 mA Load Transient at 300 mA/μS

Key Features

The switchers are capable of operating at a maximum DC current of 800 mA with peak efficiencies of 88%. The switchers are digitally programmable from 0.6V to 1.235V in steps of 5 mV. *Figures 4 and 5* show the settling time of the output being programmed to minimum (0.6V) and to maximum (1.235V). Each switcher also has an associated memory-retention LDO that can be programmed to track the switcher voltage for voltage-scaling applications, or can be used as an independent 50 mA LDO. These two memory-retention regulators can be programmed between 0.6V and 1.35V, in 50 mV steps.

The three remaining LDOs offer designers flexibility in powering other regions of the design. There are two 300 mA-output LDOs, one of which sets the I/O signaling environment for the LP5552 device, and presumably the system.

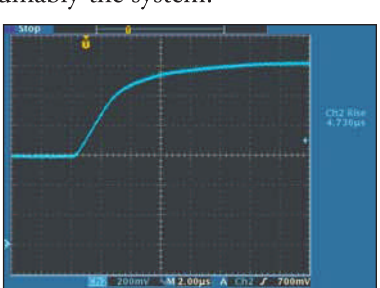

Figure 4. V_{OUT} Min to Max Settling Time with No Load

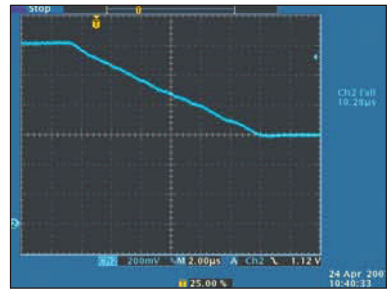

Figure 5. V_{OUT} Max to Min Settling Time with No Load

The third LDO, intended to power PLLs and/or analog functions, is capable of 100 mA of continuous output current. All of these LDOs are digitally programmable as well.

The LP5552 device has a number of additional signals to allow seamless integration of the LP5552 into the target system. ENABLE and RESETN can be used in the system to handle power sequencing, register space resets, and global power on/off. The PWROK signal is an indicator that can be used for power sequencing or power-on-reset generation. The LP5552 device also includes three GPOs that can be freely used as extra digital drivers in the system. The system designer can program them to be either an open-drain output or a push-pull output referenced to the LP5552 I/O voltage.

The LP5552 device can greatly simplify system design, minimize cost, and save PCB space. It is a very dense package that can fill most needs for a portable power system. Coupled with a PWI 2.0 master, operating in closed-loop AVS, it can realize the greatest energy savings in portable equipment. It can also be used in an open-loop DVS application, and the PWI traffic may be bit-banged from GPIOs on a processing engine without an APC. The PowerWise Interface specification can be freely downloaded and implemented at www.pwistandard.org. Information about National's PowerWise technology offerings, as well as all other power management solutions, can be found at power.national.com. ■

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pulse

INNOVATIONS & INNOVATORS

Digital POL controller turns phases on or off to suit load, increase power efficiency

When many power-supply designers hear the phrase "digital power," their reaction is often: too complicated, too expensive. Power-controller-IC manufacturers have been trying to overcome that bias by introducing digital-power-controller ICs that combine sophisticated, digitally controlled loops with ease of use, at ever-decreasing prices. Increasing power-efficiency needs are also driving system integrators to consider power efficiency along with—or even before—power-supply prices. And digital-power techniques can improve power-system efficiency along with other features, such as increased power density and nimble response to changing loads.

One new digital-power controller, Texas Instruments' UCD9240 for dc/dc POL (point-of-load) converters, packs several features that are new to digital controllers, such as multirail control for as many as eight phases and control of as many as four independent digital-control loops. These features enable improvements in energy efficiency of as much as 30% during light-load conditions by using the device's phase-management feature. Phase management allows the controller to turn a supply's phases on or off to support load fluctuations, enabling only as many phases as are required to power the load.

The chip incorporates four digital PWMs, which users configure through a GUI. The GUI allows designers to graphically, rather than algorithmically, configure power-supply characteristics, such as voltage and current thresholds and response, phase management, soft start, margining, sequencing, tracking, loop response, and fan control. The controller supports as many as 100 PMBus-interface commands for control, configuration, and management of the power supply.

The UCD9240 comes in a 64-pin QFN package for \$5.95 (1000). It is available for sampling now, and volume production will begin in the third quarter.**—by Margery Conner**

The UCD9240 digital-power controller's phase-management feature enables the power supply to operate at high efficiency over the range of the load by turning on or off power phases as the load changes.

▷**Texas Instruments**, www.ti.com.

Rugged board computer is I/O-intensive

With operation over the −40 to +70°C industrial-temperature range, the EBC-855-G-1.8-1 single-board computer from WinSystems targets rugged automation, medical-equipment, communications, security, and measurement applications. Featuring a 1.8-GHz Intel (www.intel.com) Pentium M processor and an EBX (Embedded Board Expandable) form factor, the module supports as much as 1 Gbyte of SDRAM, as much as 8 Gbytes of CompactFlash, and external floppy- or hard-disk drives. WinSystems based the EBC-855-G-1.8-1 on Intel's 855GME chip set with built-in communications and 3-D-video controllers. I/O interfaces include a 10/100BaseT Ethernet port; a miniPCI connector; four USB 2.0 ports; four serial-communications ports; AC'97 audio; and a software-programmable, 48-line digital-I/O controller.

The latest EBX single-board computer from WinSystems features a 1.8-GHz Pentium M processor and operates over the −40 to +70°C industrial range for rugged applications.

You can further expand I/O using self-stacking modules that you plug onto the PC/104 and PC/104-Plus connectors. Measuring 5.75×8 in., the module operates from 5V and typically draws 2.1A with 1 Gbyte of DDR SDRAM installed. The EBC-855-G-1.8-1 is compatible with Windows XP embedded; Linux; and real-time operating systems, such as QNX and VxWorks. Delivery is from stock to three weeks, and the list price is \$895.

—by Warren Webb

▷**WinSystems,** www.winsystems.com.

IC Manage announces new version of design-management software

Design-data management may not be the most thrilling daily task IC-design groups and their managers must perform, but IC Manage is trying to make it easier with its latest platform, IC Manage GDP (global-design platform). The small company's previous platform, IC Manage, has picked up some large clients, including Nvidia, AMD, National Semiconductor, and SMSC (www.nvidia.com, www.amd.com, www.national.com, www.smsc.com), and some great reviews from some of them (www.deepchip.com/items/0461-05.html).

The company based IC Manage GDP on the Perforce client/server-management engine, and it includes IT (information-technology) integration for hot backup, high availability, and disaster recovery, says President and Chief Executive Officer Dean Drako. It also offers revision control, configuration management, and multisite-collaboration capabilities.

Multiple trends make efficient and effective design software a must, says Drako, because the data designers' need to create a design quadruples every year. "This [increase in data] requires an increase in infrastructure, disk storage, backup, and servers," he says. Besides the need to support a growing infrastructure, a few other trends are also complicating design-data management. "People have been talking about multisite, global design for the last 10 years," says Drako. "Well, it's actually quite common now; 60% of the companies we are dealing with are doing it with design groups located here, in India, and in China. Two years ago, we didn't see nearly that many companies doing it."

More companies are also now designing around the clock, he says. "Normally, a company would do regression tests, backup, and server maintenance at night, but now, with around-the-world, around-the-clock design teams, there is no downtime. There is much less time for downtime of any kind, either due to hardware failures, software failures, backups, or disaster-recovery plans." On top of all these scenarios, Drako notes, companies, especially publicly held ones, are now putting a lot of their data on off-site storage networks to ensure compliance with the Sarbanes-Oxley, or Public Company Accounting Reform and Investor Protection, Act or for disaster-recovery compliance. "They've been putting their corporate records on these storage networks since 9/11, but they are now starting to put their design data there, too," says Drako.

The top tier of GDP is a derivative-management feature that allows design managers to track component usage for IC revisions and derivatives. When design groups are creating derivatives, the GDP tracks the bidirectional relationships between "parent" and "child." The system records sources and targets; with a set of metadata records, users can program the system to automatically propagate changes in either direction. Drako points out that conventional RCS (revision-control-system) engines typically require users to rework changes in multiple places.

The next tier is Design Assembly, which allows users to mix, match, and reuse components and IP (intellectual-property) blocks developed at any site in the enterprise and requires no scripting. The platform includes a Cross-Coupled Defect Tracking tier, in which the system records the defect and data state together. This cross-coupling, says Drako, means that designers needn't guess the design state when trying to replicate a bug. Instead, they can synchronize their work space to the exact state when someone reported, fixed, or verified the bug. The platform's next tier is Multisite Content Delivery. Design teams can push or pull common data, such as PDKs (process-design kits) and internal and external IP to any site with no delay. The platform architecture minimizes bandwidth usage and ensures that only one copy of a version travels over the WAN. IC Manage GDP also uses stateless caching that prevents the delivery of incorrect data to the remote site in the event of network disconnections or other errors.

The platform's disaster-recovery feature ensures that several copies of the configurations of design projects exist across the WAN. If, for example, your local or main data center were destroyed, a remote data center could immediately take over operation without the need for recovery from tape. The platform also supports high availability, or automatic failover, through peer-to-peer, redundant configurations. This feature allows one server to automatically take over for another in the event of hardware or other failures. Although multisite global design is common, it causes problems for IT folks to run backup on the design infrastructure because someone's always working on the system. Also with hot backup, they can do it without disturbing the work flow. With hot backup, the design database need not be in a quiescent state for backup. This feature gives design teams around the world access to their design repository across multiple time zones. IC Manage offers GDP at \$1000 to \$2000 per seat for an annual license.

—by Michael Santarini

▷**IC Manage**, www.icmanage.com.

DILBERT By Scott Adams

Not your average power analyzer, dc unit makes short work of tedious test setups

The term "power analyzer" usually describes an instrument for characterizing ac-power waveforms, measuring such properties as harmonic content. Agilent's N6705A is not such a device, however; the dc-power analyzer may well be the first product of its type. The need for it is clear; it combines the functions of a DMM (digital multimeter), an oscilloscope, an AWG (arbitrary-waveform generator), and a data logger, which design engineers commonly use together to evaluate increasingly complex dc-power systems in board- and system-level products.

In addition, the compact, rack-mountable unit accommodates one to four high-performance, modular, programmable dc-power supplies that, together, can produce an output as great as 600W. You can select these supplies from a menu of 21 module types. The AWG can modulate the module outputs at speeds as high as 160 μsec per voltage step with bandwidths as great as 5 kHz. The modulation capability also allows the instrument to generate high-power dc transients and to simulate ripple that originates with the ac line. The DMM, scope, and data logger measure output voltages and currents, and 64 Mbytes of internal memory store 30 minutes of data that the instrument captures at 50,000 readings/sec from all channels simultaneously. To capture longer records, the instrument accepts USB-memory sticks. You can also save test setups and screen images to a USB-memory stick, and you can immediately kill all output power by pressing an emergency-stop button.

For testing dc-power systems, the N6705A eliminates the need for a PC, driver software, application software, and, says the manufacturer, 90% of the effort associated with setting up an equivalent test system using stand-alone or modular instruments.

The unit eliminates the need to develop and debug programs that control a collection of instruments. All functions are available from the front panel, eliminating the need for a PC, driver software, application software, and, says Agilent, 90% of the effort associated with setting up an equivalent test system using stand-alone or modular instruments. According to a company representative, the unit's major contribution is not new measurement technology but that it enables users to more quickly get the information they require about the products they are developing than with competing technologies.

The instrument complies fully with the LXI (LAN Extensions for Instrumentation) Class C specification and includes as standard features USB 2.0, 10/100BaseT Ethernet, and IEEE 488 interfaces. A built-in server publishes a Web page from which you can remotely control the instrument over a LAN using a computer with standard browser software. The N6705A costs $6500. Prices for the power modules range from $450 to $2250 each.

Simultaneously with the N6705A announcement, Agilent also unveiled several modules for its N6700 1U (1.75-in.)-high, rack-mountable, modular, programmable dc-power system. The N6705A can accommodate all but one of the 22 N6700 modules.

—by Dan Strassberg

▷**Agilent Technologies**, www.agilent.com/find/N6705.

APACHE OPTION ADDS SUPPORT FOR ADVANCED LOW-POWER TECHNIQUES

06.07.07

EDA vendor Apache Design has added an optional module to its low-power-design tool, RedHawk-LP (low power); the new module, RedHawk-ALP (advanced low power), adds support for emerging low-power-design techniques. RedHawk-LP, which Apache introduced last year, supports low-power techniques, such as power gating and MT (multithreshold)-CMOS design. RedHawk-ALP adds support for VT (variable-threshold)-CMOS circuits with substrate back-biasing, power-gated memories, custom macros, and on-chip low-dropout-voltage regulators.

When they add the ALP option to RedHawk-LP, users can back-bias a substrate with VT-CMOS circuits, thus lowering leakage. Dynamically altering substrate voltage can add noise to the supply source and create variability problems. To address this problem, ALP allows users to extract bias networks and analyzes full-chip dynamic power integrity for trade-off analysis. The tool also comes with modeling capabilities and increased simulation support for users employing the power-gating/MT-CMOS technique on memories. Traditionally, designers have used the technique on the logic portions of the design. But they now employ it on embedded memories in SOCs (systems on chips).

Many advanced SOCs today incorporate multiple "voltage islands," or sections with different voltages. For many of these designs, users place the low-dropout voltages on-chip, rather than use an external chip. However, because these voltages serve analog functions, they tend to be somewhat temperamental. Thus, designers have traditionally used slow SPICE to simulate their behavior or used ideal voltage sources, which don't account for the power noise that low-dropout circuits generate. The ALP accurately models low-dropout circuits and gives users a true look into their impact on the rest of the SOC. The price of the RedHawk-ALP starts at $330,000.—by Michael Santarini

▶**Apache Design**, www.apache-da.com.

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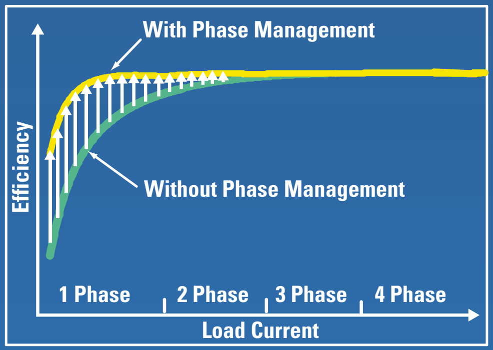
Phase Management Efficiency Benefits



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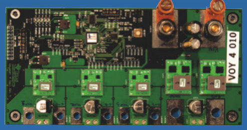

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Interop brings wave of 10GbE products

In the weeks before Interop, which kicked off on May 21 in Las Vegas, suppliers of ICs, board-level network adapters, and software released a flurry of 10GbE (10-Gbps-Ethernet)-compatible products. Without question, the technology is finding use in specialty, high-performance applications. But questions remain about when the technology will go mainstream and what role it will serve.

In the application area, little has changed since mid-2005 (see "Which interface will get traction?" *EDN*, July 7, 2005, pg 58, www.edn.com/article/CA621637). Undoubtedly, 10GbE will serve in data centers in the traditional LAN role, especially with the prevalence of rich video streams. But proponents believe that 10GbE will also usurp technologies such as InfiniBand in SAN (storage-area-network) and NAS (network-attached-storage) applications and that it will also usurp InfiniBand and proprietary interconnects in HPC (high-performance-computing) applications based on multicomputer clusters.

Ethernet-market leader Broadcom has been slow to enter the 10GbE IC market, leaving it to smaller players, such as NetEffect. However, Broadcom acquired one of those smaller players, Siliquent, in August 2005. Now, the company is rolling out a 10GbE member of its C-NIC (converged-network-interface-controller) family. In this case, "converged" implies that the ICs serve equally well in networking, storage, and clustering applications.

Broadcom's new BCM-57710 IC integrates dual 10GbE ports and includes sufficient on-chip processing to implement a TOE (TCP/IP offload engine) as well as support for iSCSI and RDMA (remote DMA). Presumably, the TOE support is necessary because host CPUs would otherwise spend too much time on the network protocol to handle the application at hand. RDMA and iSCSI, meanwhile, allow the chip to better serve cluster and storage applications. Broadcom plans to sell the IC for less than $100 (production volumes).

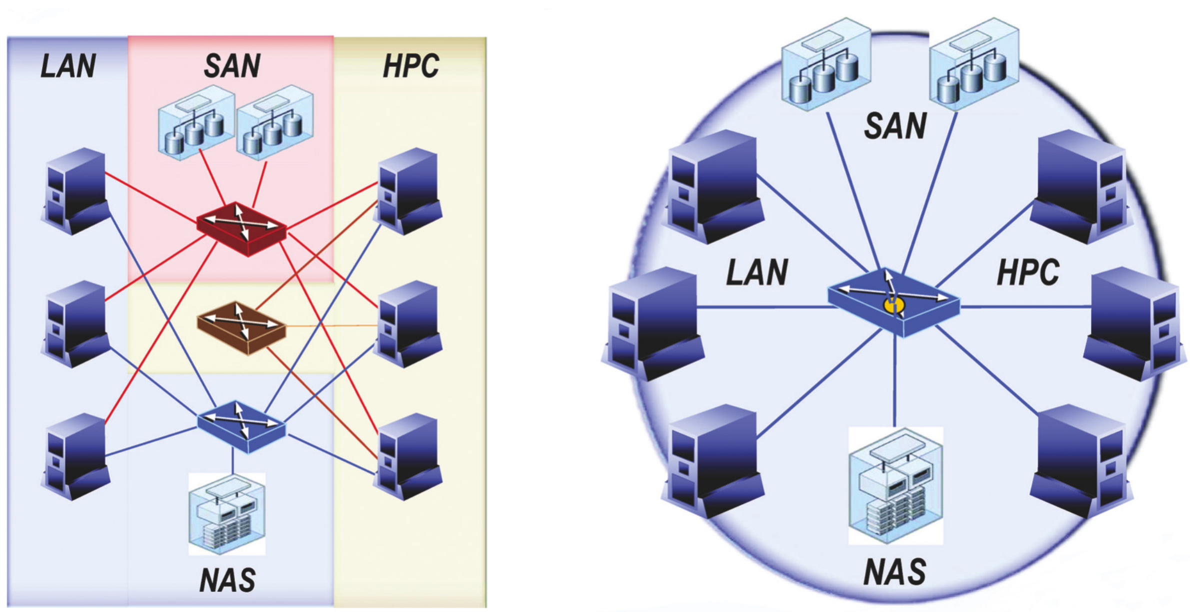
NetEffect, meanwhile, has begun to offer board-level products that host its 10GbE ICs. The market has yet to begin integrating 10GbE support on motherboards, so the company is trying to spur the market with board-level offerings. Just before Interop, the company announced the NE020 single-port board at a list price of $895.

As one might expect, though, not everyone believes 10GbE will find a market outside the LAN market. Mellanox, for instance, is still pushing InfiniBand as a better and cheaper choice than Ethernet in both clustering and storage roles. In late March, the company announced its latest InfiniBand offerings in chip and board flavors. The company lists the 10-Gbps-capable adapter boards at a starting price of less than $400. But Mellanox is ensuring its bet. The company's latest chip architecture supports both InfiniBand and Ethernet, and the company will be rolling out Ethernet and Ethernet-plus-InfiniBand chips and boards.

Not all of the Interop 10-GbE action took place in ICs. Fulcrum Microsystems, for instance, introduced the ControlPoint software suite to complement its offering of 10GbE switch chips. The development and test tools allow OEMs to quickly develop bridging, switching, and management functions and free the OEMs to concentrate on value-added features.

—by Maury Wright

▷**Broadcom**, www.broadcom.com.
▷**Fulcrum Microsystems**, www.fulcrummicro.com.
▷**Mellanox**, www.mellanox.com.
▷**NetEffect**, www.neteffect.com.



Broadcom's C-NIC ICs converge disparate and separate networks of the past (left), simplifying network layout and reducing the total cost of ownership (right).

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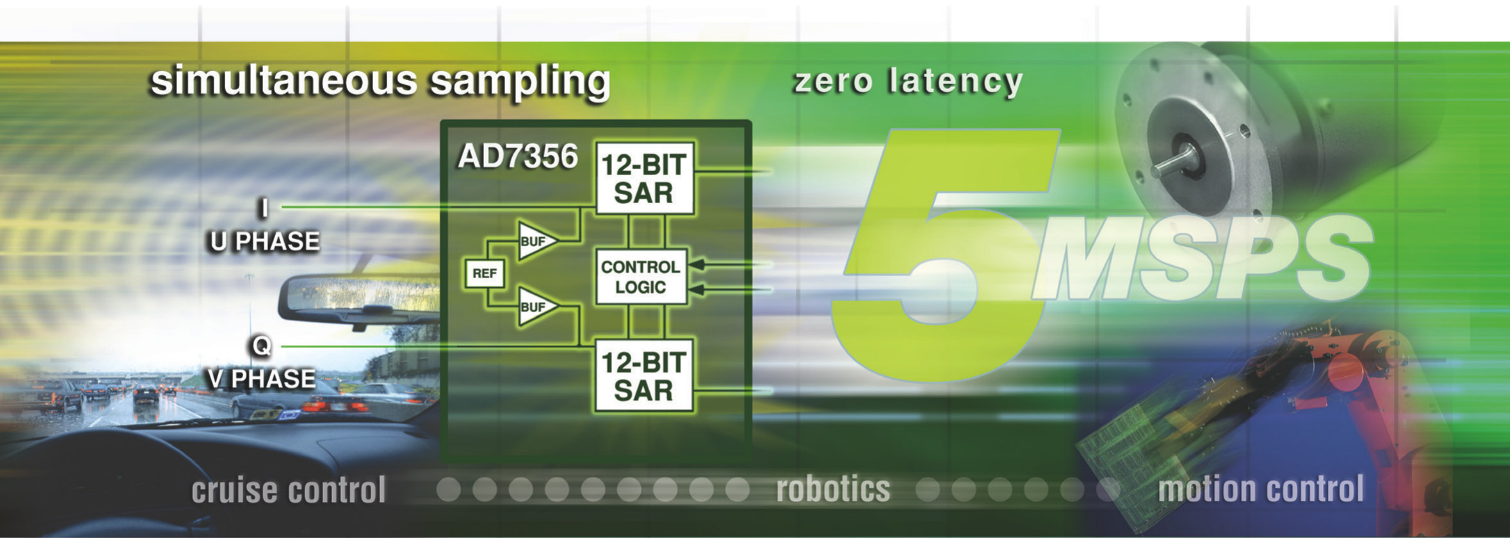

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AD7356
12-bit ADC

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- Zero latency
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- 16-lead TSSOP package
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ANALOG DEVICES

Certess tool tests verification environments

EDA start-up Certess Inc has announced the Certitude tool, which uses a mutation-analysis-software technique to help designers locate improperly functioning areas in their verification flows. "The functional-qualification tool is to verification what verification is to design, meaning that it verifies the verification," says Michel Courtoy, chief executive officer of Certess. A traditional verification environment comprises stimuli that simultaneously activate the design under test and a reference model, says Mark Hampton, chief technology officer of Certess. After it activates or exercises a problematic region of the design, it then propagates that problem area to a detection engine. The detection engine then lets the user know that it has detected a bug.

"If you don't activate the bug, if the bug doesn't propagate, or if the detection mechanism doesn't work, the bug goes to silicon," says Hampton. "Code coverage and functional coverage focus only on measuring how good the stimuli are at activating or exercising a design's behavior. Until now, verification engineers haven't had any visibility into the ability of the verification environment to propagate or detect bugs. Functional qualification spans all three aspects of the verification process. It is able to measure the ability of the verification environment to activate areas of the design, the ability to propagate potential bugs, and the ability to check them. … It gives engineers visibility into the propagation and detection."

According to Hampton, mutation analysis has been around since 1978 but has mainly been a software-research topic. "Certess is the first company to apply this technology to industrial projects," he says. He notes that research has proved mutation analysis to be effective. However, the runtimes were too long for industrial applications. Now, Certess has built a new way of applying this analysis. Users feed their Verilog or VHDL into Certitude, and the tool introduces special types, faults, or mutations in the HDL. If the verification environment can't even detect the mutations, a real error in code would also go undetected. For example, the fault A=B *and* C may replace a small bit of your code that says A=B *or* C. If your verification environment is not detecting this error, it is probably also not activating, propagating, or detecting some more complex threads in your code. Users feed Certitude test-case IDs, as well as compile-and-execute scripts that control communication between Certitude and the environment under test. The tool then outputs an HTML report that tells you the location of an unpropagated or undetected mutation.

The company has more than 50 customers for the tool, including Juniper Networks (www.juniper.net) and STMicroelectronics (www.st.com). The technology has been popular as a verification-improvement technology and as a verification-quality metric. As a verification-improvement technology, engineering teams use the tool to find weaknesses in their verification environments. If you have a fault in your design, the tool propagates to the outputs of the design through the design and shows where you injected the mutation so that you can analyze it to see what it is missing. You then must either add or fix the checker. If the mutation doesn't affect the behavior of the design and the test part, it probably indicates a condition the checker is missing or the existence of a bug or error in one of the checkers, Hampton explains.

> "Until now, verification engineers haven't had any visibility into the ability of the verification environment to propagate or detect bugs.

As a verification-quality metric, Certitude uses a statistical-sampling technique. You might, for example, have an IP (intellectual-property) block, run the metric on it, and receive a result of 87±2%. That result means that Certitude can detect that percentage of mutations in your design. You can then run the same block on different verification environments or different IP blocks on the same environment to pinpoint the location of weaknesses in your flow.

The tool currently supports Verilog and VHDL or mixed Verilog and VHDL designs. Hampton notes that the mutation-analysis technology is not language-dependent, so Certess also plans to expand it for assessing higher level verification environments, such as SystemC environments or environments that employ emulation. He notes that the tool would be ineffective for mixed-signal or analog design, because many more variables could affect those designs. Certess offers Certitude with a starting price of $100,000 for a one-year subscription.

—by Michael Santarini

▷**Certess Inc**, www.certess.com.

FEEDBACK LOOP

"Ask Intel or Microsoft to report on how many job fairs they hold in the United States and, what's more, how many over-40- or over-50-year-olds they hire. There are many of us PhDs who are unemployed or underemployed. We don't get hired as we are 'over-qualified'—code word for age discrimination. No way should the H1-B Visa program be expanded. Hire US workers first!"

—Howard Levine, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6430705. Add your comments.

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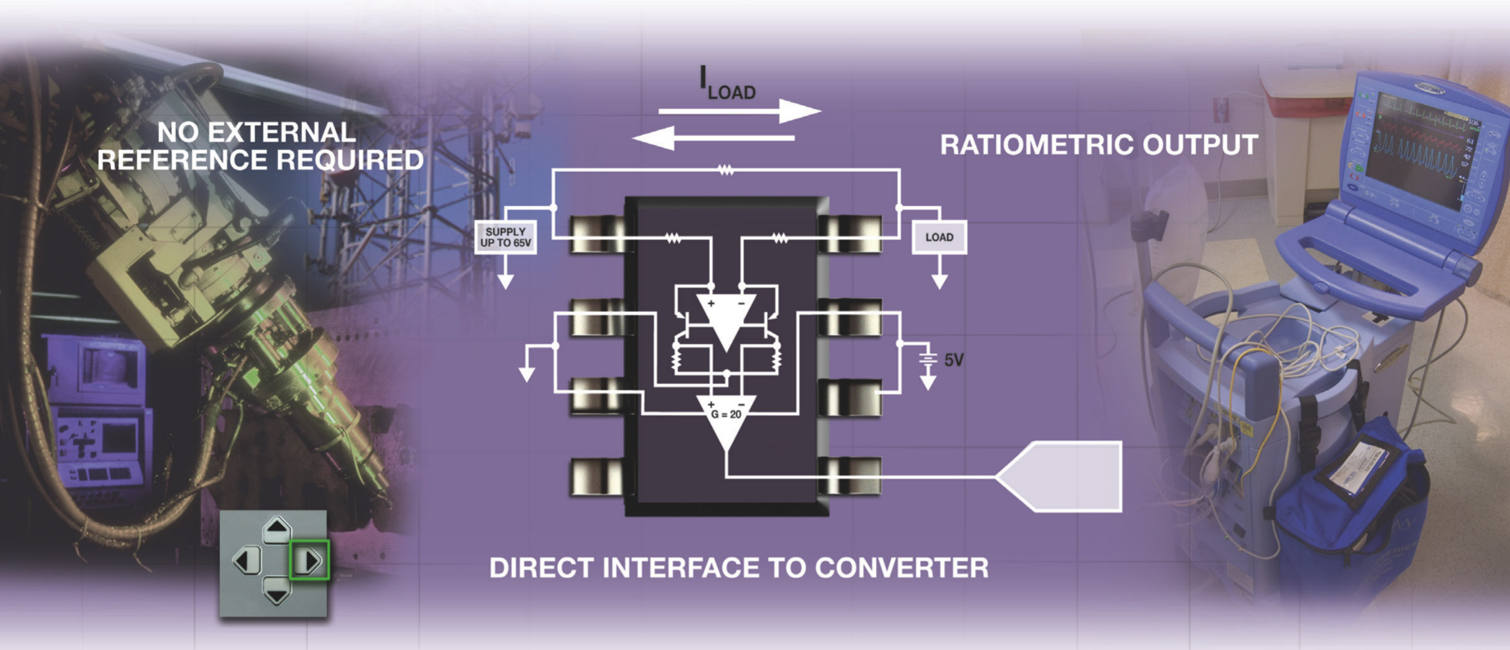

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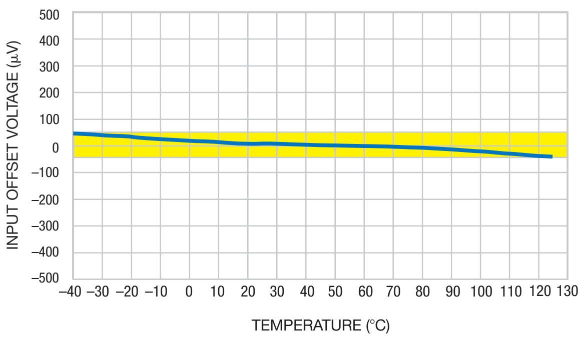

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ANALOG DEVICES

The BMW X5 is among the first automobiles to employ FlexRay networking technology.

GLOBAL DESIGNER

NXP Japan launches automotive division, targets networks

NXP Semiconductors Japan recently established the Automotive Chip Division and the Competence Center to support chip development for Japanese automotive manufacturers. The company also disclosed that it is developing a chip to integrate multiple automotive networks in cooperation with an unnamed Japanese automotive manufacturer. NXP Semiconductors, a spin-off of Royal Philips, is a global IC player, and the Japanese operation has focused on the automotive market as a major target market. The Automotive and Identification divisions provide half the total revenue of NXP Semiconductors Japan, although the company does not publicly disclose sales of the Japanese organization. Because analysts predict that the semiconductor market for automotive applications will continue to grow at a rate of 20% annually, NXP has strengthened the automotive-semiconductor business by integrating the sales, marketing, and R&D departments.

Hiroyuki Hamada, general manager at the Automotive Division, points out three growth areas, including the car-entertainment market, encompassing radio, audio, information/connectivity, and navigation/vision. The company plans to develop and supply chips essential for home-server connections to automobiles using Wi-Fi and other wireless networks. The connectivity will support automotive music players and digital radio.

The second target area centers on the safety and comfort market. The company has developed security technologies, such as vehicle-immobilization schemes and various sensors. And the company expects in 2007 to ship 45 million RFID units for tire-pressure sensors. The company's other sensors feature detection of wipers and throttle angles. Shipment of sensor chips into ABS (antilock-braking-system) applications has surpassed 300 million units. "One of two motor cars uses our sensor chips," Hamada says.

Networking is the third target area. In the networking market, the company will offer transceiver chips for high-speed CANs (controller-area networks) and FlexRay networks, both standard interconnects for automotive applications. The company supplies a chip set combining the NXP TJA1080 FlexRay transceiver with a fail-safe SBC (system-basis chip) to BMW in Germany for use in the X5 car. The IC serves in the electronics that implement active roll stabilization and electronic-damping-control functions.

Hamada also discloses that NXP will combine its expertise in a number of networking technologies in an upcoming chip. The company currently offers networking chips based on the CAN and LIN (local-interconnect-network) standards and will integrate that support into a chip that also supports FlexRay. NXP has partnered with a major Japanese automotive manufacturer on the multinetwork chip.

The automotive focus has also yielded The Competence Center, an engineering organization dedicated to chip development for tier-one auto manufacturers. The company will place Japanese engineers in customers' global sites to provide on-site development help.**—by Takatsuna Mamoto, Editor in Chief, *EDN Japan***

▷**NXP Japan**, www.nxp.com.

PLUGFEST MOVES MOBILE WIMAX TOWARD INTEROPERABILITY, BROAD DEPLOYMENT

06.07.07

The mobile flavor of WiMax (Worldwide Interoperability for Microwave Access) could be the keystone leading the wireless broadband technology to widespread deployment. Mobile WiMax supports true mobile broadband and will likely take over the fixed-location market, as well, due to economies of scale (see "WiMax gains in mobile-broadband game, but 4G lurks," *EDN*, March 29, 2007, pg 56, www.edn.com/article/CA6426878). To push interoperability among Mobile WiMax products, key players gathered in Sophia Antipolis, France, in mid-May for the third public Mobile WiMax PlugFest.

AT4 Wireless, a Málaga, Spain, services and testing company and the ETSI (European Telecommunications Standards Institute) hosted PlugFest. In attendance were a number of key semiconductor, communication-equipment, handset, software, and test-equipment vendors, including Alcatel-Lucent, Fujitsu, Intel, Motorola, PicoChip, Samsung, Agilent, Azimuth Systems, and Rohde & Schwarz.

PlugFest marked the first time that the WiMax Forum tested key mobility features, such as MIMO (multiple input/multiple output) and beam forming. Such technologies will be key to Mobile WiMax's realizing its range and performance goals. PlugFest also focused on session handover between two base stations.

—by Maury Wright

▶**AT4 Wireless, www.at4wireless.com.**

▶**ETSI, www.etsi.org.**

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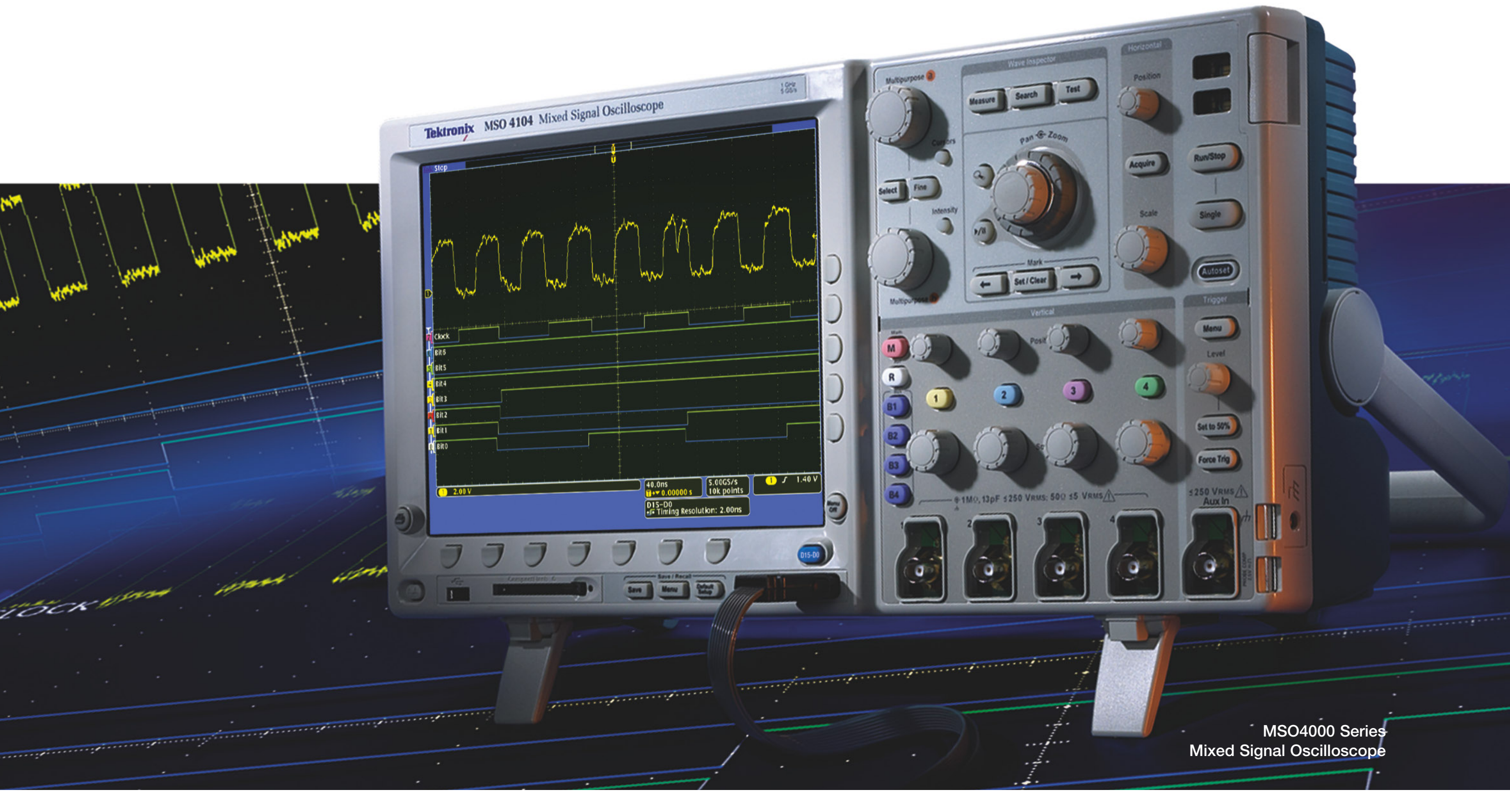

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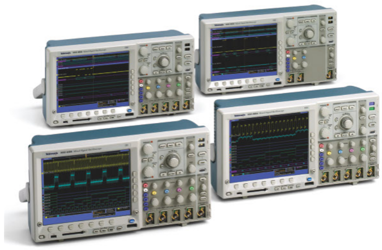

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BY BONNIE BAKER

Where did all the bits go?

Theoretically, the SNR (signal-to-noise ratio) of an ADC is equal to (6.02N+1.76) dB, where N equals the number of ADC bits. Although I'm a little rusty with my algebra skills, I think that the SNR for any 16-bit converter should be 98.08 dB. However, I see something different when I read converter data sheets. For instance, the specification for a 16-bit SAR (successive-approximation-register) converter can typically be as low as 84 dB and as high as 95 dB. Manufacturers proudly advertise these values on the front page of their data sheets, and, frankly, an SNR of 95 dB for a 16-bit SAR converter is competitive. Unless I am wrong, the 98.08 dB I calculate is higher than the 95-dB specification that I find with the best of the 16-bit-converter data sheets. So, where did the bits go?

Let's start by finding out where this ideal formula, 6.02N+1.76, comes from. The SNR of any system, in decibels, is equal to 20 $\log_{10}$ (rms signal/rms noise). When you derive the ideal SNR formula, you first define the rms signal. If you change a peak-to-peak signal to rms, you divide it by the $2\sqrt{2}$. The ADC rms signal in bits is equal $(2^{(N-1)}\times q)/2\sqrt{2}$, where q is the LSB (least-significant bit).

All ADCs generate quantization noise as a consequence of dividing the input signal into discrete "buckets." The ideal width of these buckets is equal to the converter's LSB size. The uncertainty of any ADC bit is ±1/2 LSB. If you assume that this error's response is triangular across each bit, the rms value equals this LSB signal's magnitude divided by $\sqrt{3}$: rms noise$=\pm(\text{LSB}/2)/\sqrt{3}=q/\sqrt{12}$.

Combining the rms-signal and rms-noise terms, the ideal ADC SNR in decibels is:

$$\text{SNR} = 20\log_{10}\left(\frac{\left(2^{(N-1)}\times q/2\sqrt{2}\right)}{q/\sqrt{12}}\right) = 6.02N + 1.76.$$

Again, where did the bits go? The ADC vendors enthusiastically explain the missing-bits phenomenon, because they bench-test their devices to see how good the SNR is. Fundamentally, they find that the device noise from resistors and transistors creeps into the results. Vendors test their ADC SNR by inputting their data into the following formula:

$$\text{SNR} = 20\log_{10}\frac{\text{RMS SIGNAL}}{\text{RMS NOISE}}.$$

These theoretical and tested SNR formulas are complete, but they provide only part of what you need to know about how many bits your converter is truly giving you. THD (total harmonic distortion), another ADC specification you need to watch, is the ratio of the rms sum of the powers of the harmonic components, or spurs, to the input-signal power: $\text{THD}_{\text{RMS}}=20\log_{10}\sqrt{((10^{\text{HD2}/20})^2+(10^{\text{HD3}/20})^2+(10^{\text{HD4}/20})^2+\ldots)}$, or

$$\text{THD}_{\text{RMS}} = 10\log_{10}\left(\frac{P_S}{P_O}\right),$$

where HDx is the magnitude of distortion at the Xth harmonic, P_S is the signal power of the first harmonic, and P_O is the power of harmonics two through eight. Significant ADC INL (integral-nonlinearity) errors typically appear in the THD results.

Finally, SINAD (signal-to-noise and distortion) is the ratio of the fundamental input signal's rms amplitude to the rms sum of all other spectral components below half of the sampling frequency, excluding dc. The theoretical minimum for SINAD is equal to the ideal SNR, or 6.02N+1.76 dB, with SAR and pipeline converters. For delta-sigma converters, the ideal SINAD equals 6.02N+1.76 dB+10 $\log_{10}(f_S/(2BW))$, where f_S is the converter sampling frequency and BW is the maximum bandwidth of interest. The not-so-ideal value of SINAD is $-20\log_{10}\sqrt{(10^{-\text{SNR}/10}+10^{+\text{THD}/10})}$, or

$$\text{SINAD} = 10\log_{10}\frac{P_S}{P_N + P_D},$$

where P_S is the fundametal signal power, P_N is the power of all the noise spectral components, and P_D is the power of all the distortion spectral components.

So, the next time you're looking for lost bits, remember that it is the combination of SNR, THD, and SINAD that gives you the complete picture of the real bits in your ADC—regardless of whether it's SAR, pipeline, or delta-sigma technology and regardless of the number of bits that the first page of the data sheet mentions. EDN

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Bonnie Baker is a senior applications engineer at Texas Instruments and author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie@ti.com.*

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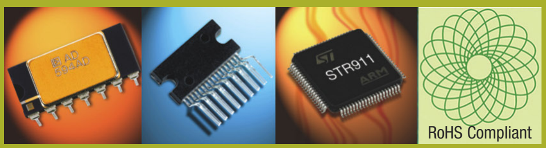

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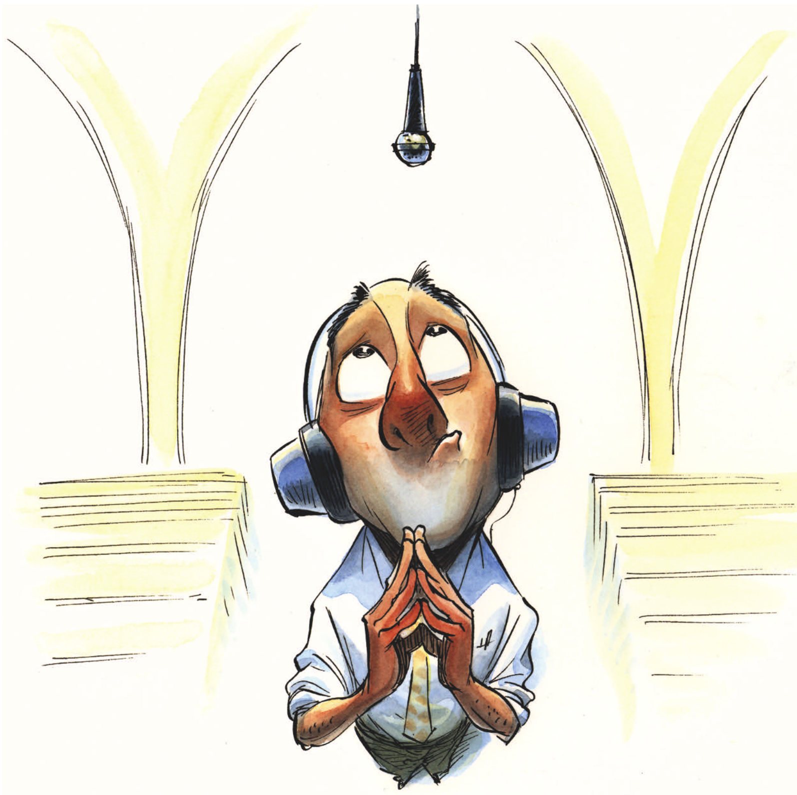


DANIEL VASCONCELLOS

The "cube" in this tale was the sound booth at Springfield Assembly of God Church (Springfield, VT), where I'm the sound man. We have an electret microphone hanging from the sanctuary ceiling that covers most of the room. This mic became completely unusable because of severe electrical noise. Due to the inconvenience of accessing the mic and the partial coverage that two other mics afforded, I put off the project until I had a Sunday afternoon with nothing else pressing. We missed the overhead mic, though, for recording, for hearing-impaired people using wireless earphones, and for picking up someone speaking near the back of the room.

We'd had similar noise problems in the past that we resolved with contact cleaning, so I tried cleaning the contacts on the mic and its connector. No change. I brought the mic down to the sound booth and plugged it into the board with a short cord to investigate the problem. There was still a buzz, but it wasn't nearly as bad as with the mic near the ceiling. It sounded like noise from the light dimmer in the booth, and turning off the light confirmed my suspicion. I turned it back on. Touching the end of the microphone had little effect on the buzz, but covering the end with my hand considerably reduced it. Just waving my hand over the end of the microphone had a dramatic effect on the noise, as long as I was grounded by holding the mic in my other hand. The microphone was obviously sensitive to electrostatically coupled noise.

Some change either in the microphone or in its noise environment caused the problem to manifest. I put the mic back in its place under the ceiling and turned off the ceiling lights. Quiet! I turned on the paddle fans. There was a familiar slight buzz, the origin of which had been a mystery until now. I asked our pastor when he'd replaced the incandescent lights with compact fluorescent lamps, and it sounded like that event about coincided with the onset of the severe noise problem. Reverting to incandescent lights was an unpalatable option; the pastor is also an accountant, and he'd done the math.

We had multiple noise emitters and one receiver. A single-point solution would be simplest. The effectiveness of placing my hand between the microphone and the dimmer-controlled light circuit in the sound booth was encouraging. A Faraday cage grounded to the microphone shell should be sufficient. I wanted to avoid altering the directional pattern and thought a spherical shield would have the least impact, but making a small sphere out of flat screening was impractical. I made a cylinder, closed at one end, out of window screening. A mounting ring that I fabricated from polyvinyl-chloride pipe and drilled for three Sheetrock screws would hold the cage, and the screws would electrically connect it to the microphone shell. I spray-painted the whole assembly black to match the microphone, then removed the paint from the electrical contact areas.

Back at the church, I sandpapered the anodizing off the microphone shell where the screws would touch it, then attached the shield and put the microphone back up. Complete silence! The noise was inaudible, and whatever happened to the microphone's directional pattern was an improvement. I can now use the sanctuary microphone without having to pad down the speaker that's right behind it. EDN

Dick Neubert has been an electronics enthusiast since he was 6 years old. Like Dick, you can share your Tales from the Cube and receive $200. Contact Maury Wright at mgwright@edn.com.

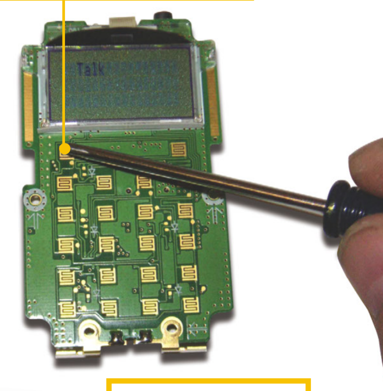
PRY FURTHER AT EDN.COM

Go to www.edn.com/070607pry for additional images of the Polycom CT12.

Breaking up: diagnosing a dropped phone

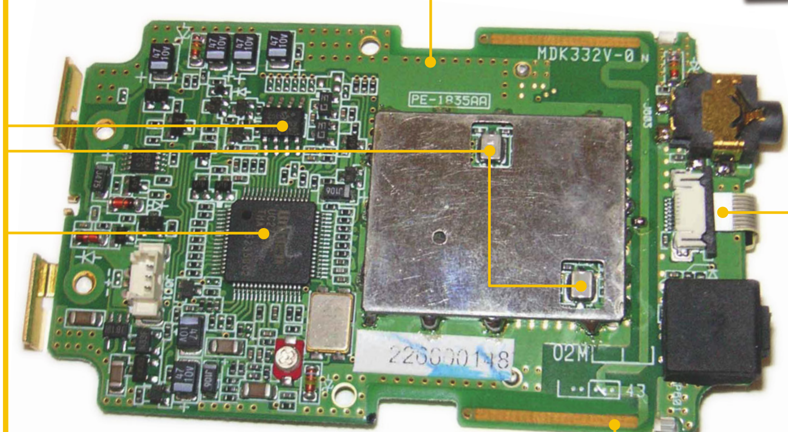
About to hang up from a conference call, I accidentally dropped Plantronics' (www.plantronics.com) Polycom CT12 portable phone. It just happened to hit the floor right on its headphone plug, breaking its solder joints. I guess the fall did more damage, because, shortly thereafter, I noticed that its audio was intermittent, so I dismantled the phone, revealing a clean, modern design. The PCB (printed-circuit board) takes up the entire phone, which works without the case—albeit with audio interference. You can more easily design, test, and repair the phone when it is without its case. The designers of the phone also addressed cost in the design phase, during which 80% of cost requirements occur. To fix the audio problem, all I had to do was touch a soldering iron to the five solder pads on the surface-mounted headphone connector. I wondered whether the solder joints would have broken if Plantronics had used a though-hole headphone jack as opposed to a surface-mounted one. The Plantronics phone, including headset, costs $70.

The phone's PCB is a complete product; to make it work, you need only to hook up the battery and touch the keypad. Some pulsating audio interference disappears when the board is in the case–a shielding component that is not essential to the function of the product. The plastic or a conductive coating inside the case most likely contains a conductive fiber to reduce RFI (radio-frequency interference).



Via stitching creates multiple low-impedance ground planes in the PCB, which has a gold-immersion finish, not just for ROHS (reduction-of-hazardous-substances) compliance, but also to prevent oxidation on the pushbutton contacts. The manufacturer soldered the charging terminals to the board, but mounting screws running through holes in the brass terminals take up the mechanical strain on the PCB's terminals.

A large metal can shields the RF components and dominates the PCB. The case has two cutouts to allow the use of components that are taller than the metal case. A 64-pin Uniden (www.uniden.com) UC2746C quad gull-wing baseband chip lies outside the metal can. A low-profile crystal oscillator sits next to the baseband chip to minimize clock-trace length. The double-layer, 31-mil-thick PCB also includes a 32-kbit Microchip (www.microchip.com) 24LC32A serial I^2C EEPROM. Another eight-pin IC, most likely a regulator or battery charger, resides near the battery connector.



The connector for the LCD screen sits near the dipole antenna. The short ribbon cable has eight circuits. The length ensures a minimum of stray radiation from the cable.

Emerging from under the metal can, a dipole RF antenna has size and spacing that comply with the 2.4-GHz operating frequency of the DSSS (direct-sequence-spread-spectrum) phone. Plantronics removed the solder mask from the radiating areas of the antenna. A via at the extremity of each arm of the dipole connects to an identical trace on the other side of the board. Each of those traces then returns to the ground plane.

"A predictable supply of power, protected
from faults, is an essential ingredient of an efficient,
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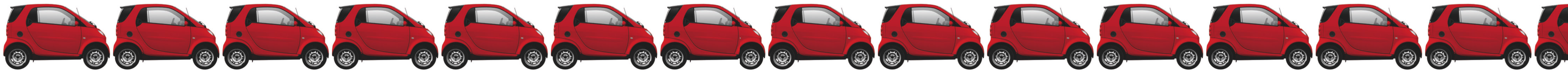

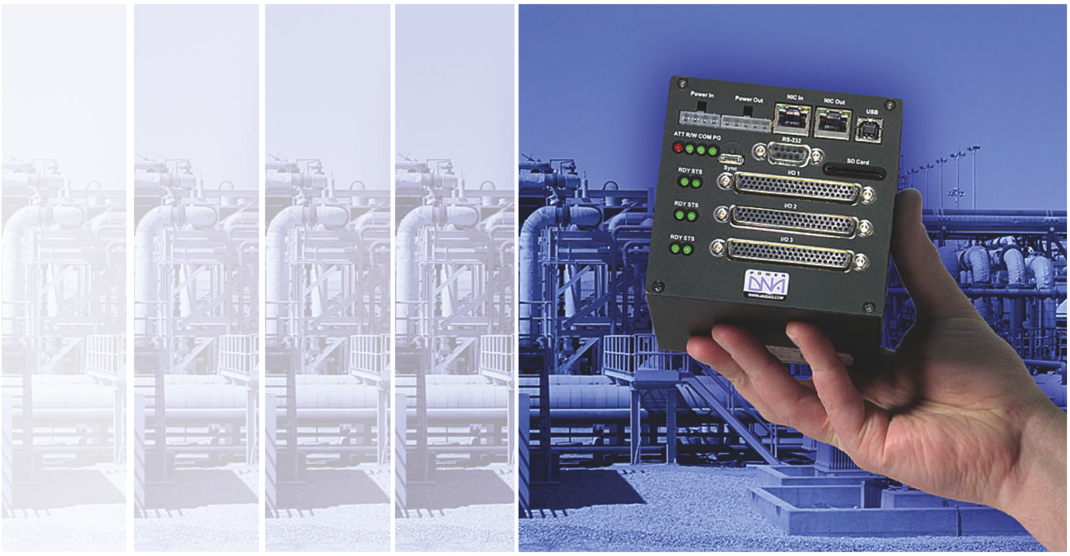

Figure 1 The UEIModbus Cube data-acquisition and -control interface communicates with the host system using the Modbus protocol.

Industrial networks *mix old with new*

BY WARREN WEBB • TECHNICAL EDITOR

INDUSTRIAL DEVICES AND THEIR INTERCONNECTIONS HAVE AN EXTENDED LIFE CYCLE REQUIRING DESIGNERS TO INTERACT WITH MULTIPLE GENERATIONS OF TECHNOLOGY.

As distributed, intelligent devices become commonplace in industrial-automation, process-control, and building-management applications, the number of techniques designers use to connect them has multiplied. Industrial designers confront the prospect of dozens of field, sensor, control, and device buses, each with a different communications protocol, to interface, control, and remotely monitor new embedded devices. Although the design of a new industrial-automation system and network would be an exciting assignment, most designers face lower budget projects and process improvements that must interface and operate with various versions of legacy technology.

You can trace modern industrial interconnections almost 50 years to the 4- to 20-mA analog-current-loop standard for instrumentation, which, not surprisingly, designers still widely use. A current loop has several advantages in an industrial setting: The signal is immune to most electrical interference, only two wires provide the supply voltage and monitoring current, the 4-mA offset of the base current makes it simple to detect open cables, and a current signal can transmit over long distances. By the mid-'80s, designers were looking for digital-data exchange to take advantage of remote computer control and system optimization. This need led to a proliferation of digital-bus structures for communications among sensors, actuators, controllers, and office-based enterprise computer systems.

Engineers based most early digital-interconnection schemes on serial communication because they understood it well, they could easily write interface software for it, and it was available in

every microprocessor. Although it defines no standard protocol for communicating over the network, the RS-485 specification, with its differential-line drivers and receivers plus an allowable node separation of 4000 feet, became the industrial designer's favorite digital interconnect. Industrial-device vendors then developed several hundred proprietary control-bus architectures based on RS-485 multidrop or similar physical hardware. Each architectural standard claimed to solve some unique environmental, data-rate, timing, or network-media problem.

These vendors based most of these early communications methods on bus architecture to reduce wiring and installation costs because one bus can support multiple nodes on a single twisted pair as opposed to individual pairs. This reduced complexity also results in lower maintenance costs and two-way communications, and it leads to standardized, off-the-shelf products. However, digital-communications networks have several inherent problems. In general, they are more susceptible to noise, cost more per node, may be slower, and work with a multitude of standards that are not interoperable. Although many of the early bus names survive, most of their developers have restructured those buses to deliver higher data rates, more nodes, real-time response, and reduced environmental interference.

GOING DIGITAL

Modbus, which debuted in the late 1970s, was one of the first digital-communications protocols to connect industrial PLCs (programmable-logic controllers) with a host computer or other PLCs. The Modbus architecture allows the host to read or load digital- and analog-I/O-signal registers in the remote controller. With new physical layers, such as Ethernet, fiber, and wireless, Modbus continues to be the most widely used control bus in industrial applications. For example, United Electronic Industries recently released the UEIModbus Cube, a data-acquisition and -control interface that communicates with a host computer or PLC using Modbus TCP (Transmission Control Protocol) over Ethernet (**Figure 1**). The UEIModbus 600 Cube measures 4×4×5.8 in. and supports as many

AT A GLANCE

- New industrial designs must interoperate with legacy systems employing current-loop and low-data-rate serial communications.
- Vendors have updated the early digital-networking standards that still dominate the industrial landscape, such as Modbus and Profibus, to match today's technology.
- Featuring ubiquitous availability, open standards, lower costs, and higher speeds, Ethernet challenges many industrial-networking standards.
- With low-cost hardware and simple installation, wireless networks fit many industrial-monitoring and distributed-control applications.

as 150 analog inputs or 288 digital-I/O channels. Targeting monitoring and control applications in severe industrial environments, the cube delivers an operating-temperature range of −40 to +85°C and can withstand 50g of shock and 5g of steady vibration. Prices for the Modbus TCP 600 Cube start at $1795, and it is now available.

With roots in Germany, Profibus is the most widely accepted international standard for deterministic communications among industrial-automation devices. The developers of Profibus based it on a real-time token-bus architecture with multiple master or slave devices and a variety of hardware formats, operating-system drivers, protocols, and application interfaces. Profibus PA (process automation) enables both the data communication and a power source for two-conductor applications, such as industrial sensors and actuators. You can connect as many as 32 field devices to a Profibus PA bus segment. Profibus DP (decentralized periphery) targets applications requiring high speeds and low connection cost and can be a replacement for conventional parallel communications or the 4- to 2-mA current loop. The Profibus DP has a maximum data-transmission rate of 12 Mbps, and you can connect as many as 126 field devices to a Profibus DP bus segment.

Targeting the huge installed base of current-loop systems, the HART (Highway Addressable Remote Transducer) communications protocol offers designers a digital industrial-automation protocol that communicates over 4- to 20-mA analog-instrumentation wiring. HART is both an analog and a digital protocol in which both the 4- to 20-mA current and the combined digital signal are valid output values from the device. For example, Moore Industries International offers a family of two-wire, loop-powered Smart HART temperature and signal transmitters with input-to-output analog accuracy as high as ±0.014°C (**Figure 2**). The 4- to 20-mA temperature-output signal also has a superimposed HART digital signal, which allows any HART-compatible control device to program zero, span, sensor-trim offset, and other calibration variables and to interrogate and read multiple real-time process variables. Using this protocol, you can link as many as 15 transmitters through a single twisted-pair wire.

To respond to the requirement for increased performance and nearly instan-

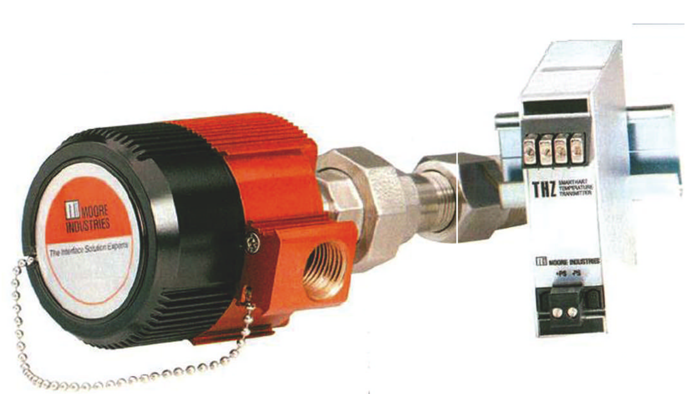

Figure 2 Smart temperature transmitters from Moore Industries combine the 4- to 20-mA temperature-output signal with a superimposed HART digital signal.

Figure 3 The ioLogik E2240 uses Ethernet communications for active status reporting of attached sensors, transmitters, transducers, and valves.

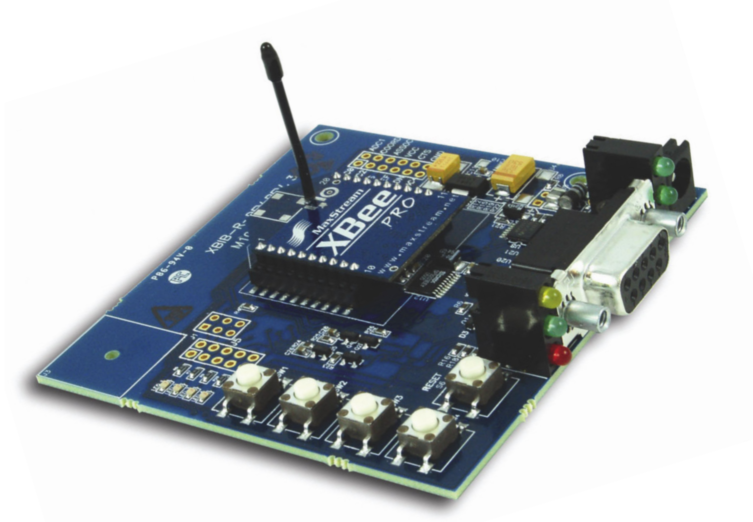

Figure 4 The XBee OEM RF-module-development kit from Maxstream provides the tools to experiment with multiple ZigBee wireless-network topologies.

taneous metrics, many industrial designers are turning to Ethernet. Although it is not a perfect fit for automation systems, Ethernet has a number of advantages over industrial-control buses. It is an open standard with multiple vendors competing to produce the lowest cost and most flexible products, and many organizations have Ethernet experts available from the enterprise network. However, coupling Ethernet with a control protocol still involves problems in the industrial environment. Ethernet is a shared-media interface with rules to handle simultaneous data-transfer requests and ensure that the system loses no data. A collision results when two Ethernet nodes attempt to transmit at the same time. Nodes must then wait a random time interval and attempt to retransmit the data. As the amount of traffic increases on the network, the number of collisions increases. Because a node may have to retransmit data and the time required to reach the destination is variable, Ethernet networks are nondeterministic.

SPEED WINS

Although determinism is a major operational issue at the control level, 100-Mbps and 10-Gbps Ethernet is considerably faster than most proprietary buses, so that, even with collisions, network speed is not a problem. Another technique engineers use to live with a nondeterministic network is to reduce the traffic on the network segment. An intelligent switch in place of a hub divides networks into smaller, faster segments by examining data packets and forwarding only those with the proper address. Reduced network traffic results in fewer collisions. Segmenting the network also helps in situations in which operation must continue even with hardware failures.

The ioLogik E2240 from Moxa Technologies exemplifies a stand-alone, remote I/O server that uses Ethernet communications for active status reporting of attached sensors, transmitters, transducers, and valves (**Figure 3**). Unlike most other Ethernet-based industrial-automation devices that require the host computer to continually poll for the status of each I/O device, the E2240 I/O server intelligently sends status information only under specified conditions. This report-by-exception approach reduces the load on the host CPU and network resources. The unit includes eight 16-bit voltage or current analog inputs plus two 12-bit analog outputs. On the control side, the E2240 supports Modbus TCP, TCP/IP (TCP/Internet Protocol), and several other Ethernet protocols. An onboard RS-485 serial interface supports the Modbus/RTU (remote-terminal-unit) protocol. The E2240 is available now for $550.

As installation, retrofit, and maintenance costs escalate, designers are also considering wireless communications for industrial-networking applications. Thousands of industrial applications require a reliable, wireless-communications network to provide acceptable performance and reduced cost. Although parameters vary from application to application, several common design requirements characterize industrial wireless networks. Most applications call for a large number of sensor or control nodes; therefore, simplified and low-cost hardware is essential. Because vendors may deploy network nodes in remote and inaccessible locations, a long battery life is also one of the primary objectives. Although low-cost nodes translate into reduced processing resources and simplified software, users still expect secure and reliable data transfers in the harsh RF environments of many industrial applications.

Designers can arrange industrial wireless networks in multiple configurations for optimum performance, as they can with the networks' high-bandwidth counterparts. For example, a point-to-point wireless bridge connects two endpoints and simply replaces a communica-

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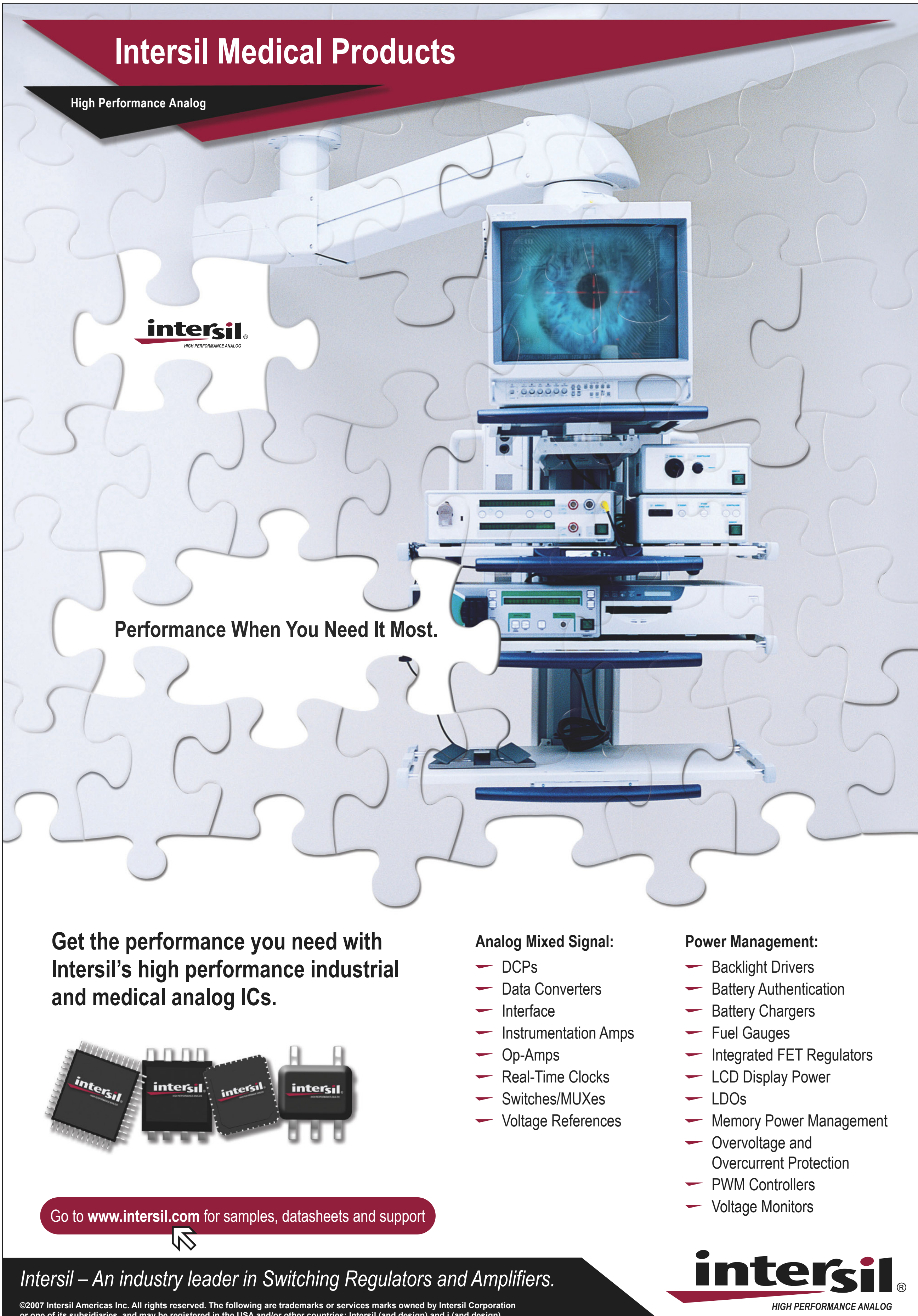
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tion cable. Designers can use a point-to-point wireless link to connect a remote-control panel to a movable device, such as a robot to eliminate the tethered cable. Many low-data-rate, point-to-point links incorporate low-cost transceivers at each end that translate a common standard communications protocol, such as RS-232. Another wireless-network format, point-to-multipoint, includes a central base station and multiple wireless nodes in a star or hub-and-spoke pattern. A third wireless format—low-power, multihop mesh networks—processes messages by passing packets from node to node until the message reaches its destination. Unlike a point-to-multipoint network node that filters out all packets except its own, a mesh-network node receives and retransmits packets addressed to other nodes. A multihop network operates much like the Internet and provides redundant communications paths from source to destination. If a path stops working due to hardware failure or interference, a mesh network automatically reroutes packets through an alternate path.

WIRELESS STANDARDS

Providing a standard for ultralow-power, low-data-rate networks, IEEE 802.15.4 defines a wireless-network architecture for many smart industrial applications. Operating in the unlicensed frequency bands, the standard defines the PHY (physical) layer and MAC (medium-access-control) sublayer specifications for low-rate devices communicating at 20 kbps in the 868-MHz band, 40 kbps in the 915-MHz band, and 250 kbps in the 2.4-GHz band. Transmitters use both DSSS (direct-sequence spread spectrum) with BPSK (binary-phase-shift-keying)- and O-QPSK (offset-quadrature-phase-shift-keying)-modulation techniques. Designers using this architecture can arrange networks in multiple topologies, and the technology provides addressing for more than 65,000 nodes. Adding to the PHY and MAC layers that the IEEE 802.15.4 defines, the ZigBee Alliance defined the remaining layers for low-rate, low-power wireless applications. Various network-layer data-delivery strategies allow system designers to trade communications frequency for battery life in remote nodes.

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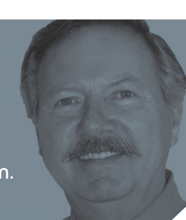
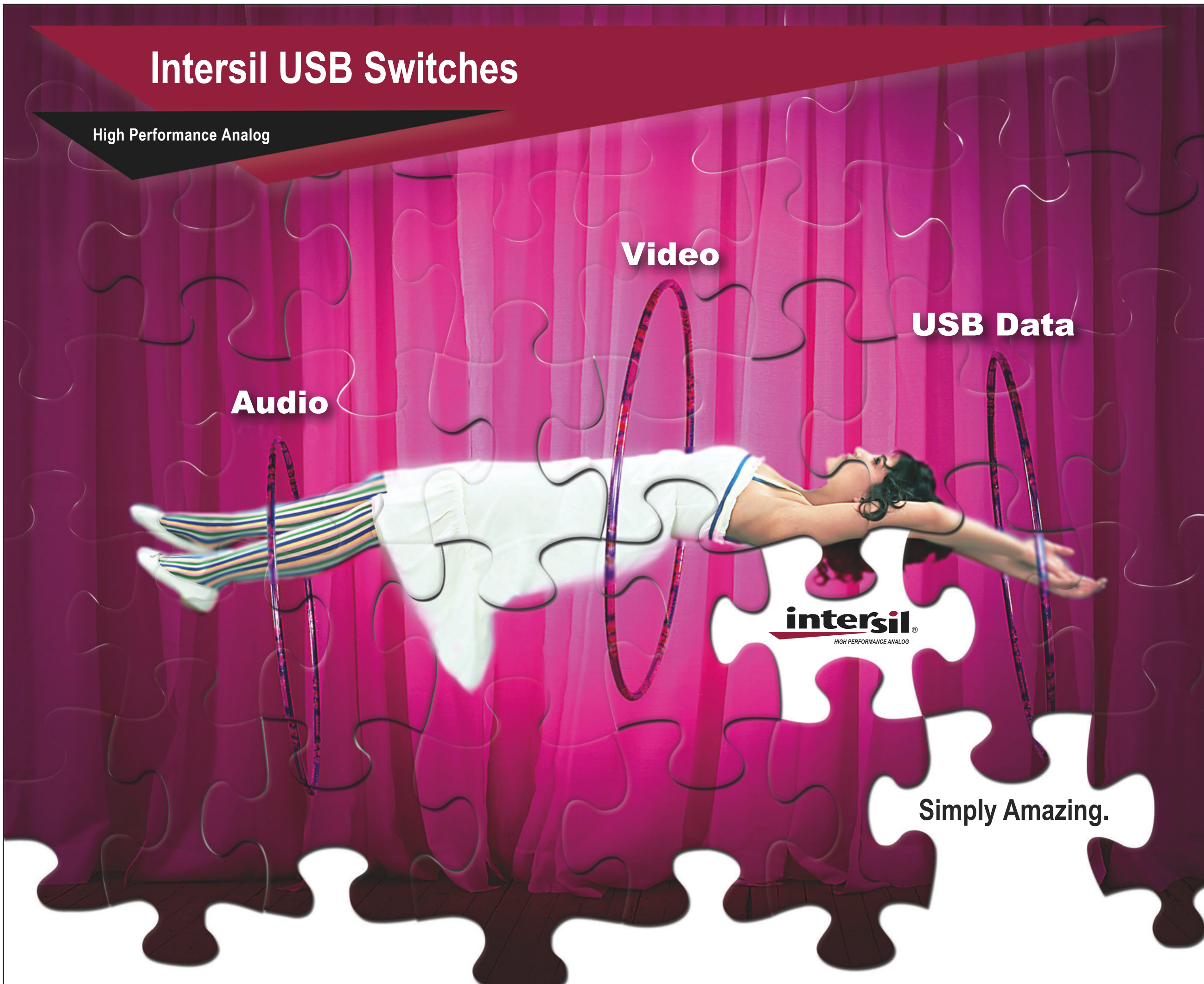
Very-low duty cycles allow nodes with coin-type batteries to remain operational for years.

The ZigBee- and IEEE 802.15.4-compliant XBee OEM RF module from Maxstream targets low-cost, low-power wireless-sensor-network applications. The XBee module operates within the 2.4-GHz frequency band and delivers 1 mW of transmitting power for a range of 100 to 300 feet. The unit employs DSSS modulation in peer-to-peer, point-to-point, point-to-multipoint, and mesh-network topologies. Rated for the −40 to +85°C industrial-temperature range, the module transmits data at rates as high as 250 kbps. The XBee OEM RF module sells for \$19 and is available now. Development kits are also available for \$339 (**Figure 4**).

Because of the longevity of industrial-automation equipment and its associated networking schemes, updated technology takes years to supplant legacy devices. During the transition, designers must devise clever techniques and workarounds to deliver the benefits of modern industrial automation and maintain compatibility with currently available systems. Although new projects are favoring Ethernet or wireless technologies in an effort to lower system costs, industrial-system designers can expect to interface their latest creations with ancient current-loop and serial communications for the foreseeable future. **EDN**

You can reach Technical Editor Warren Webb at 1-858-513-3713 and wwebb@edn.com.





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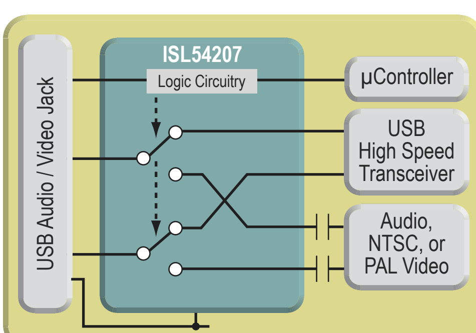
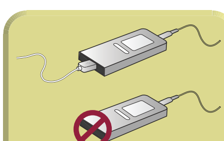
ISL54417	0.007	12	0.04 / 0.03





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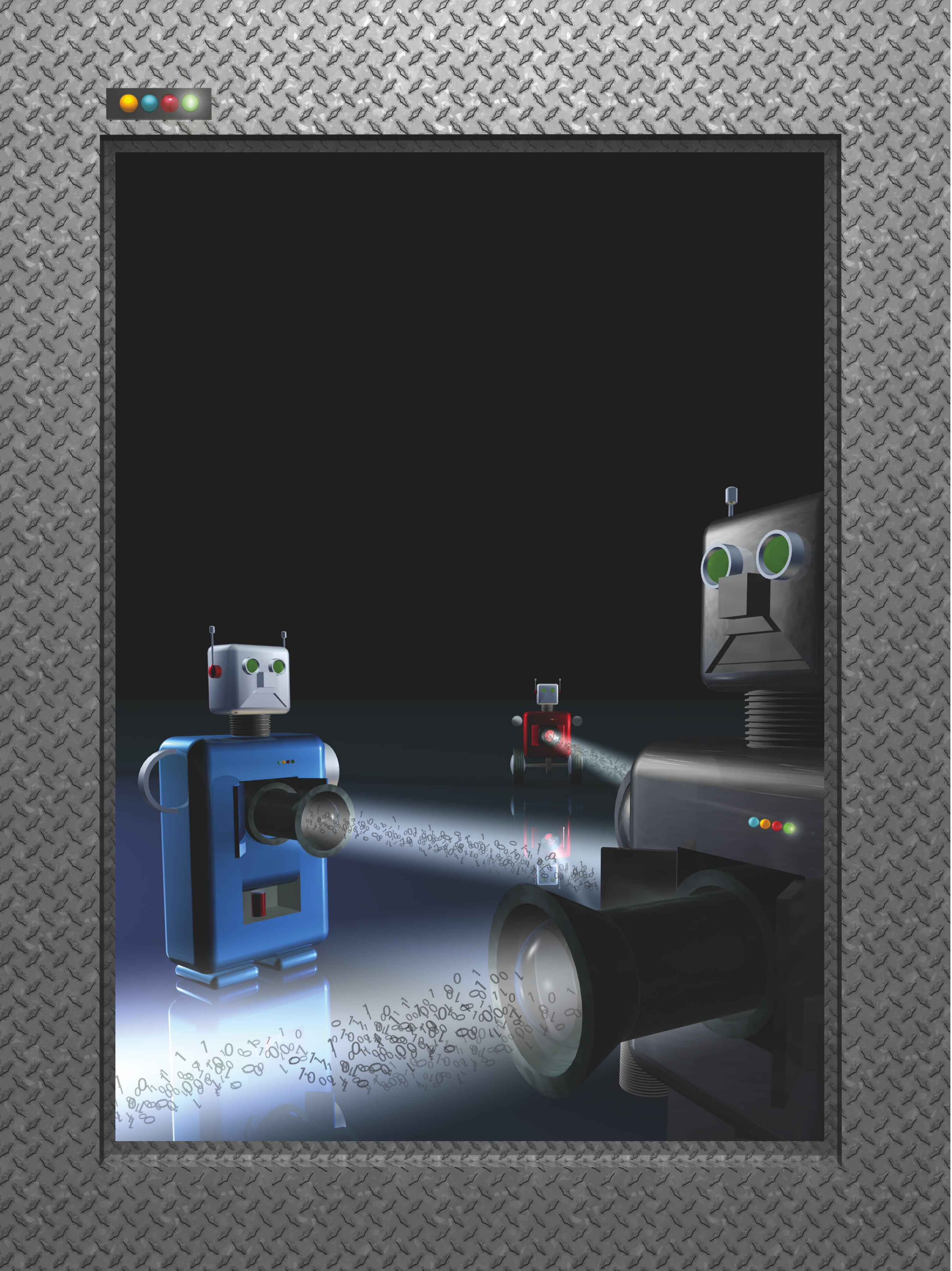

HOP, JUMP, AND SPREAD: WIRELESS MACHINE-TO-MACHINE INTERFACES

PAUL RAKO • TECHNICAL EDITOR

INEXPENSIVE WIRELESS LINKS AND EMBEDDED PROCESSORS COMBINE TO SUSTAIN THE COMPUTER REVOLUTION. THESE DEVICES CAN'T DO EVERYTHING AT ONCE, THOUGH. RADIO AND SYSTEM DESIGN IS ALWAYS AN ANALOG DISCIPLINE.

Wireless machine-to-machine interfaces represent the third wave of computers. The first wave was business computers, expensive mainframe and supercomputers affordable only to the largest businesses. This phase appeared and grew during the 1960s and 1970s. The second wave of computers started in 1981 when IBM introduced the PC. This period flourished in the 1980s and 1990s. The new millennium has given rise to the third wave of computers, during which decreases in cost and advances in technology allow a machine as prosaic as a toaster to have an embedded processor as well as a wireless radio. These processors provide utility when they stand alone but add even more value when they can communicate among themselves without human intervention. With the advances in small, cheap computers, advances in wireless technology have also appeared. The advent of wireless-cell-phone techniques has spearheaded these advances. These techniques include wireless networks for cell phones and burgeoning Wi-Fi-hot-spot phenomena (**Figure 1**).

Although M2M (machine to machine) is the current marketing buzz word, the precedents for wireless-M2M technology arose decades ago. One term that has fallen out of favor is "telemetry." The early space program used radio telemetry for sending data from a spacecraft back to NASA and control signals to the spacecraft—all without human intervention. The availability of military-frequency allocations eased NASA's task. High power levels ensured reliable communications. More recently, designers have applied the concept of space telemetry to more worldly vehicles, such as Formula 1 race cars. On-board computers can send data from the car to a trackside computer that then automatically adjusts the air-to-fuel ratio and other parameters to achieve the best performance. Other wireless-networking applications include vending machines with cell phones inside that

AT A GLANCE

- Machine-to-machine wireless networks primarily use cell-phone or ISM (industrial/scientific/medical) bands.
- WiMax (Worldwide Interoperability for Microwave Access) and 700-MHz analog-TV bands will provide new frequencies.
- FHSS (frequency-hopping spread spectrum) hops the frequencies; DSSS (digital-sequence spread spectrum) smears frequencies, and agile radios jump frequencies looking for a clear band.
- Battery life and interference are big issues in wireless networks.
- Careful system design minimizes interference and maximizes battery life.

"call home" when the machine runs low or when a need for service arises. In the automotive world, the term "telematics" has replaced the old-fashioned word "telemetry." Telematics covers entertainment, navigation, and emergency uses. General Motors has pioneered this concept with its OnStar service. OnStar includes a powerful cell phone with a car's entertainment and navigation systems. It can download real-time traffic reports, and it allows users to report emergencies or request assistance. Because the cell phone receives its power from the car battery and because the antenna need not fit into a tiny handheld phone, the ability of the system to connect almost always exceeds the ability of a handheld cell phone to connect.

Because M2M wireless networks represent convergence among several emerging technologies, such as spread-spectrum wireless, embedded processors, and network-routing protocols, an abundance of hype surrounds the market. The hype touts the fact that a wireless network will allow communication between a light switch and a refrigerator. However, that idea is the result of a grand vision that drives M2M. Internet pioneer Tim Berners-Lee states: "Machines become capable of analyzing all the data on the Web—the content, links, and transactions between people and computers. A 'Semantic Web,' which should make this possible, has yet to emerge, but when it does, the day-to-day mechanisms of trade, bureaucracy, and our daily lives will be handled by machines talking to machines, leaving humans to provide the inspiration and intuition" (**Reference 1**). The scope and perception of this comment cement Berners-Lee's reputation as a genius and big-picture thinker. The problem comes from the fact that no one knows what the killer application will be for wireless M2M networks. Although this fact may not worry Berners-Lee and others, a lot of unsolved issues remain between the dream of wirelessly connected machines and the engineering to achieve this goal.

The futurists and pundits envision an M2M network with machinery that connects to the Internet. The problem with that scenario is that it requires the embedded system in the machine to have not only a radio, but also the protocol stack and hardware for TCP/IP (Transmission Control Protocol/Internet Protocol). This situation brings up the problem of assigning IP addresses for all these gismos and then providing DNS (domain-name server) or some other means to find and use these devices. Panasonic builds its network cameras with a hard-IP address to a server that the company operates. When you buy the camera, you can navigate to that site with your browser, and the server can then establish the routing between your camera and your browser. This approach is a bit clumsy at best. Some researchers have proposed just randomly assigning an IP address to every piece of equipment (**Reference 1**). They point out that IPv6 (IP Version 6) provides for 2^{128} addresses, enough to put 6.6×10^{23} devices on every square meter of the Earth.

A large swath of wireless M2M networks will exist on the Web as subnets, often without routing or IPs. To get data from the Web to this subnet, you need to install a router and a gateway. All these realities conspire against the hype that wireless-M2M-network nodes will cost less than $2 each and will all connect to the Web. Full-blown computers in their own right, routers and gateways will offset the low costs of any network node. Only a few years ago, people thought that Bluetooth was going to remove every cable from your car, desk, and benchtop. But, in reality, Bluetooth serves as a wireless-headset enabler with a range of two feet—from your belt to your ear. The realities of wireless networking include the large cost of writing and standardizing the high-level protocols for these devices to find and connect to one another. Once engineers achieved that goal,

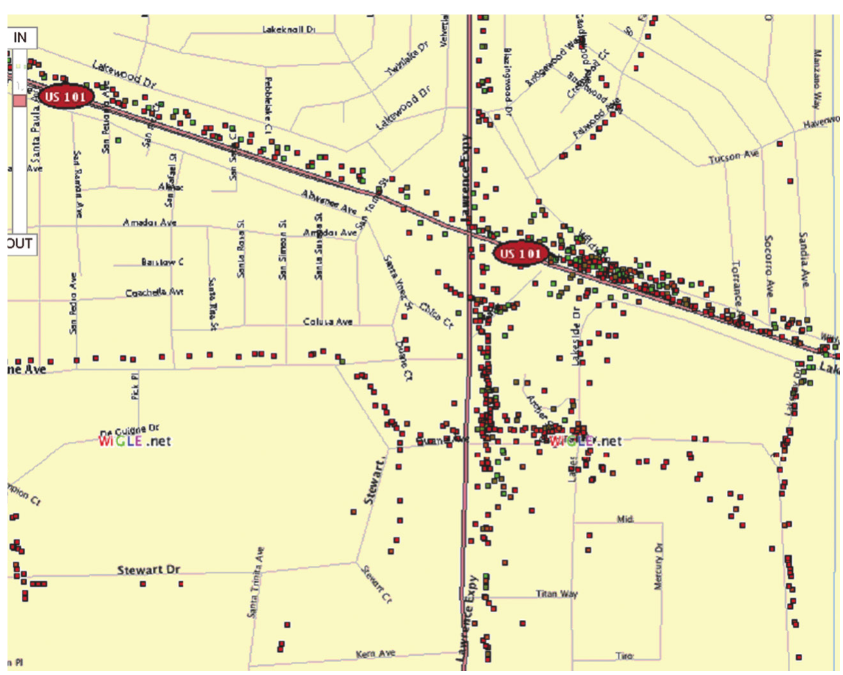

Figure 1 Wireless hot spots are becoming so prevalent that they line the roadways of many towns (courtesy WiGLE.net).

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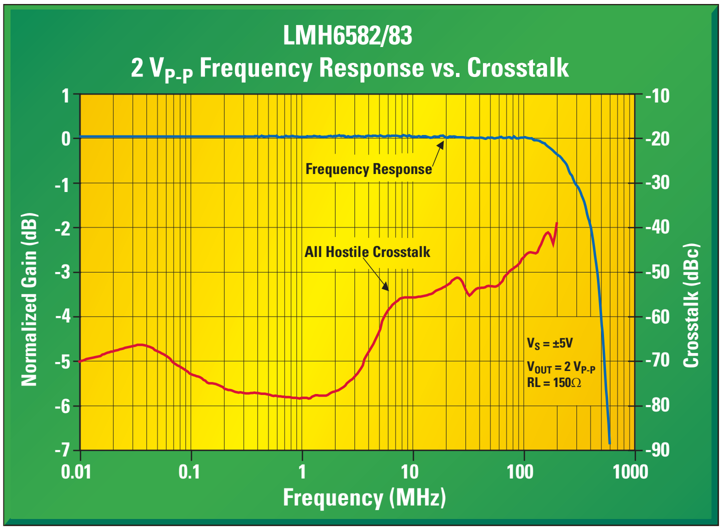

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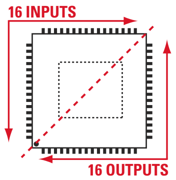

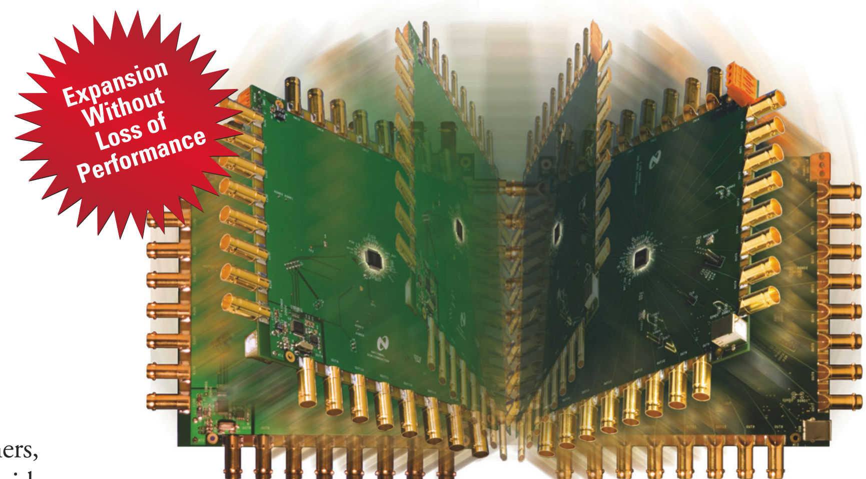

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they realized that these devices needed security; otherwise, anyone could pry into your PDA or cell phone. Any wireless M2M system that claims to be ad hoc or self-arranging must address all theses issues. These delightful laboratory curiosities are less useful in a world of teen-agers intent on vandalizing your data just for the sheer, destructive fun of it all.

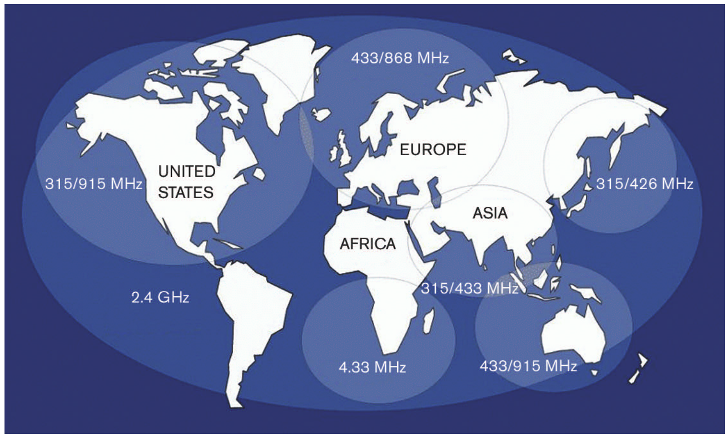

Figure 2 Wireless devices can work worldwide at 2.4 GHz. Geography limits other frequency bands (courtesy Texas Instruments).

Let's examine what M2M wireless networks are and are not. M2M wireless devices currently use either the older cell-phone or the burgeoning ISM (industrial/scientific/medical) network, which uses the 800-MHz, 900-MHz, and 2.4-GHz bands. In the near future, however, the WiMax (Worldwide Interoperability for Microwave Access) network, which runs licensed in the 10- to 20-GHz range and unlicensed in the 2- to 11-GHz range, will dominate. Both cell-phone companies and computer giants, such as Intel, are also looking longingly at the analog-TV bandwidth of 50 to 200 MHz. The low frequencies of these bands allow them to achieve longer ranges with less power; further, rain and fog do not affect their reception. Despite the surge of WiMax, it is still a technology of the future. Today, the two predominant wireless technologies are cell phones and IEEE 802-style ISM.

Cell-phone networks have the advantage of long reach and pervasive deployment. Many field-application engineers had difficulties trying to find wireless IEEE 802 hot spots until their companies gave them Verizon and AT&T PC cards that connect to the Web through the cell-phone system. They can now check e-mail from almost anywhere in the United States. M2M networks that use the cell-phone network will enjoy those same benefits. As a result, mobile and remote applications, such as OnStar and trucking fleets that monitor vehicles' positions by tying a GPS (global-positioning-system) receiver to a wireless module, have gravitated to cell-based connectivity. This feature helps fleet owners analyze routes and also has the Big Brother ability to check on drivers' behavior. Similarly, a bridge structure may have sensors that monitor stress, traffic, and degradation. These sensors can connect to maintenance and highway-control computer systems and provide emergency alerts when an earthquake or an accident, for example, compromises the structure. The downsides of these cell-phone-based systems are cost and power consumption. The cost of the wireless modules is declining rapidly due to the ubiquitous consumer cell phone, but the cost of using the network is still relatively high due to the telecom companies' predatory pricing models that charge for connections or minutes when an M2M system often needs to send only a few bytes of data.

Figure 3 Wireless 802.11 hot spots in New York are close enough to interfere with each other (courtesy WiGLE.net).

The other M2M networks, IEEE 802 types, operate in the familiar ISM ranges of 800 MHz in Europe, 900 MHz in the United States, and 2.4 GHz worldwide (**Figure 2**). In addition, proprietary networks can operate in other frequency bands, such as 434 MHz, which garage-door and keyless-entry remotes use, as well as in medical bands for more reliable communications. The most familiar standard for this type of network is ZigBee. It uses standardized protocols to allow small, battery-powered devices to communicate. Some ZigBee proponents claim that batteries using the technology have lifetimes approaching 10 years, but a five- or even a two-year lifetime is more realistic. The biggest problems with these networks are interference and battery-life issues. Because the 2.4-GHz band is unlicensed, there are no restrictions on how many transmitters can reside in any one area (**Figure 3**). Some proponents claim that several 802-style networks can coexist, but the success of the networks is also their failure. If the world becomes rife with 2.4-GHz transmitters, the effective radius of communication will likely decrease to a few feet, and, even then, this technology can severely affect data rates. *EDN* Senior Technical Editor Brian Dipert noted this phenomenon in testing a wireless-speaker system (**Reference 2**). The use of the wireless speakers causes his 802.11 wireless Wi-Fi (wireless-fidelity) LAN either to stop working or to achieve the connection at 50% data rates.

Despite concerns regarding interference, some successful M2M applications use these ISM wireless protocols. Verifone's POS (point-of-sale) terminals use Connect One's iChip IP-controller chips so wireless LANs can connect to a credit-card company to authorize a pur-

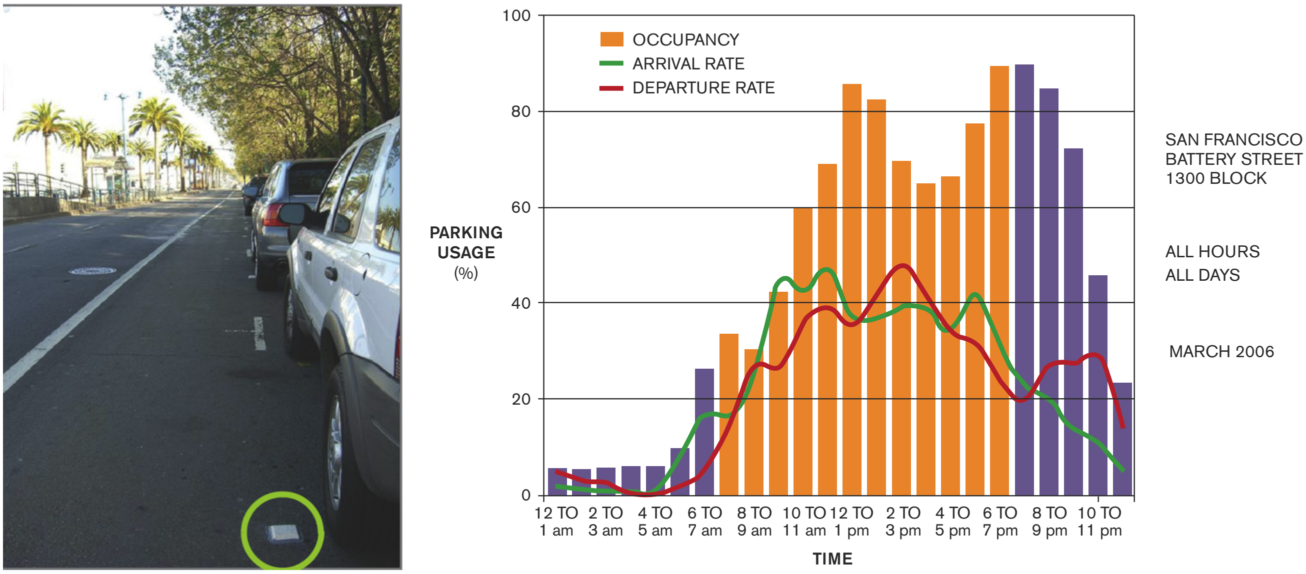

Figure 4 Streetline Networks puts wireless sensing in this parking bump to detect the presence of a car (a). It checks parking-meter compliance and directs drivers to empty spots (b) (courtesy Streetline Networks).

chase. The benefit is the speed of transaction. It takes many seconds for an embedded modem to dial a phone number, connect, establish the communications, establish the encryption, and get the authorization for a 16-digit credit-card number. A wireless system can more quickly perform these tasks and needs no phone lines or Ethernet connections to the cash register. Because they use a network connection, all the cash registers in a large store can simultaneously access the credit-card-authorization server rather than wait for an open phone line. This technology is a good fit in areas in which fast payment is a real benefit, such as fast-food counters and subway-ticket kiosks. In these scenarios, the cash registers all have IP addresses and all hook up to the Internet.

Having the devices directly on the Internet is not always necessary or advisable, however. ZigBee proponents are looking to connect tens, hundreds, or even thousands of sensors to a central node, or coordinator. You can install a gateway if you need to send data to or receive data from the Internet. Although the ZigBee network is not a conventional subnet, it does use packet routing and other sophisticated techniques to route the data among peer devices and to central coordinators. Classic ZigBee applications are HVAC (heating/ventilation/air conditioning) and lighting control in buildings and data collection in factories or fields. One ingenious application uses ZigBee nodes embedded in the reflector bumps on roads (**Figure 4**). These nodes can monitor and report parking-space usage in real time and allow collection of data to verify whether people are feeding the parking meters (**Reference 3**). Although some industry participants include RFID schemes as wireless M2M networks, others see the technologies as distinct markets.

Figure 5 Actress Hedy Lamarr invented and patented the concept of frequency-hopping-spread-spectrum radios in 1942 (courtesy Mischief Films).

To better understand the features and drawbacks of wireless M2M networks, remember that analog-design principles apply in two critical areas: the actual radio communications of a network and high-level-system design. In this regard, you cannot combine all the claims of all the marketing people and expect your system to perform at that level. Advances in high-speed CMOS may make a $2 radio feasible, but that radio is a ZigBee-style 802.15.4 radio, not a radio that can use cell-phone networks. Furthermore, if you want the wireless device to be on the Internet, you must pay for a processor big enough to hold a TCP/IP stack and provide for a way to assign and route IP addresses. In the same vein, vendors often talk about long battery life. Wireless devices in a mesh network pass data from end devices to the periphery of the mesh. That ability impacts the battery life of devices more central to the mesh. In addition, an ad hoc network must spend a considerable amount of resources identifying and incorporating new devices into the net. If a device cannot route along an established mesh path, then it must negotiate and establish a new path. All this work uses up battery resources. Worse yet, battery use need not be uniform across the net, meaning that some devices will need battery replacement sooner than

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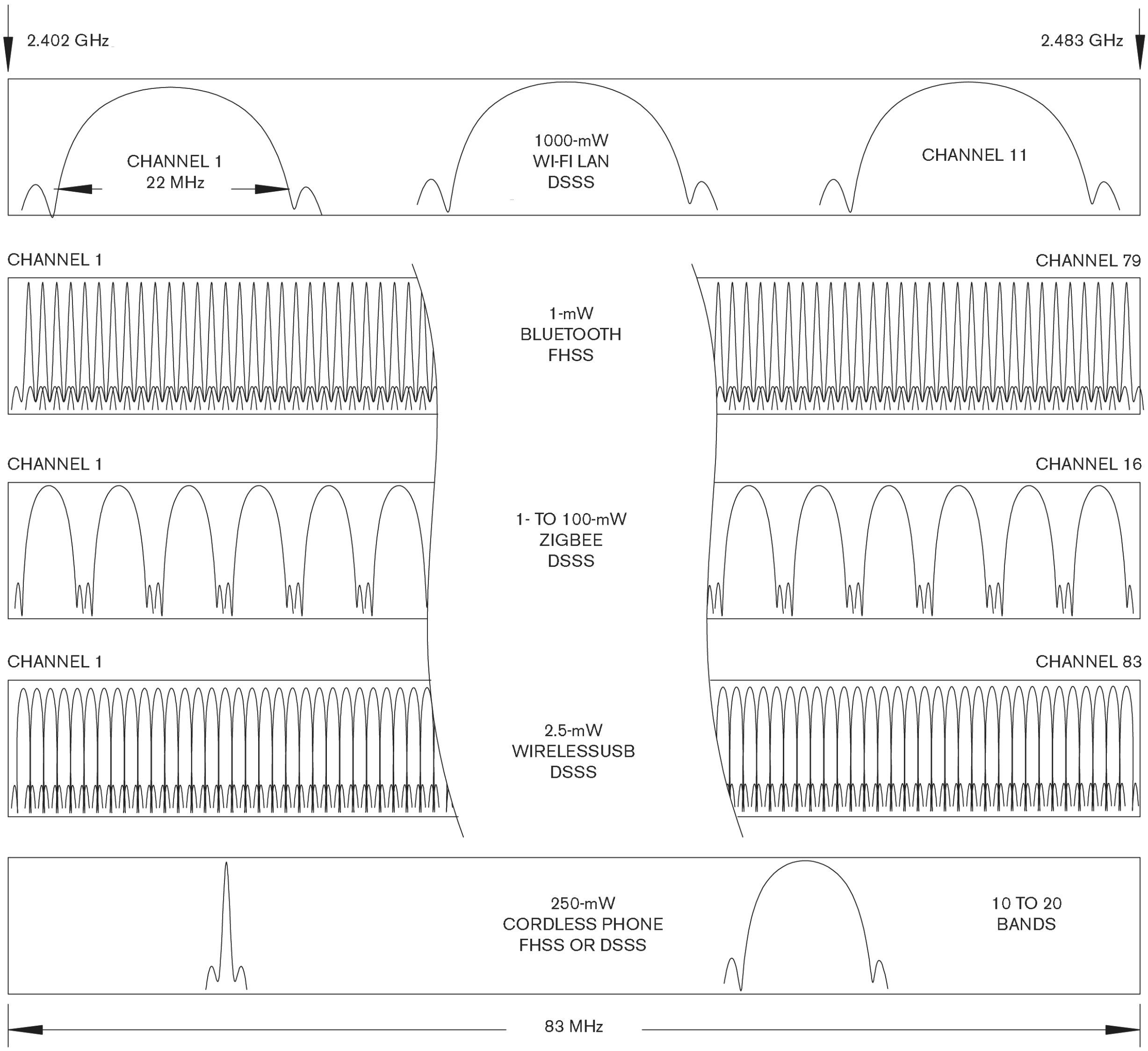

Figure 6 The 2.4-GHz ISM band has many radio standards that cannot coexist or may interfere with each other. There are 11 Wi-Fi bands, but only three do not interfere. The DSSS modulation code that Wi-Fi uses cannot prevent interference from other Wi-Fi transmitters at the same frequency.

others. Or, more likely, users will discard partially discharged batteries because system-maintenance procedures will dictate replacing all the batteries in the mesh at periodic intervals based on the worse device's battery consumption.

Further, ZigBee-network devices operating at 2.4-GHz worldwide bands can transmit data at 240 kbps, those using the 915-MHz US ISM band communicate at only 40 kbps, and those using the 868-MHz European ISM band communicate at only 20 kbps. So, although you may want to move your devices out of the crowded 2.4-GHz band, the slower data rates may cost you in shorter battery life.

Cell-phone wireless networks may give you "everywhere" connectivity, but they don't provide "always connected in real time" connectivity. A reliable connection may use proprietary networks and frequencies, meaning that you cannot ride the low-cost coattails of the ZigBee-design protocol. Smart, self-healing devices that form ad hoc networks may not be the least expensive. And as always, factors including interference, network topology, and device protocols have an adverse effect on battery life.

THE BAD NEWS

Spread-spectrum techniques do not result in infinite available bandwidth. These techniques let transmitters share bandwidth, but each additional transmitter reduces the data rate of the other transmitters, their range, or both—that is, if all the transmitters use the same protocol. The 2.4-GHz ISM frequency band provides a striking example of how interference can make all the devices on the band useless (**Reference 4**). The license-free ISM bands by design contain interference sources. The developers of the unlicensed, 2.4-GHz band established it because microwave-oven magnetron tubes operate at this frequency. These ovens have a small but measurable impact on wireless interference. More troubling, in-

ductive heating and molten sulfur lighting provide even more non-communications-related interference in this band. These interference sources are of concern, but permitted uses of the 2.4-GHz band are so numerous that connections are becoming unreliable in some areas because the FCC (Federal Communications Commission) and other regulatory agencies allow many protocols. These protocols include FHSS (frequency-hopping spread spectrum), which the Bluetooth protocol employs. Actress and communication-technology inventor Hedy Lamarr invented frequency-hopping radios as she played along to a player piano (**Figure 5** and **Reference 5**). During World War II, she figured out that secret radio communications would benefit the war effort. She conceptualized that the receiver could hop along the same pattern as the transmitter did as it hopped to different frequencies, just as her fingers could hit the same keys that the player-piano roll was hitting. This realization led to the idea that radios could communicate with each other while preventing eavesdropping.

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The Bluetooth protocol divides the 83-MHz-wide, 2.4-GHz ISM band into 79 1-MHz slices. The Bluetooth devices then hop among 32 of these frequencies at a maximum rate of 1600 hops/sec. Two collocated Bluetooth devices could interfere with each other only 1/79 of the time. When this situation happens, the high-level protocols request that the system retransmit the lost packets. If the Bluetooth device hops into the frequency of your ZigBee or Wi-Fi LAN, it will also interfere with those devices.

Consumers' insatiable need for bandwidth drove the 802.11b standards that provide 11-Mbps speeds. These systems use the DSSS (digital-sequence-spread-spectrum) technique, in which the radio uses 22 MHz of the 83-MHz to 2.4-GHz ISM band. A PRBS (pseudorandom-binary-sequence) phase modulates the frequency across the band. Unlike FHSS, DSSS continually shifts rather than hops the discrete frequencies. Cellphone implementations of DSSS allow multiple transmitters to operate on the same band. Unfortunately, the 11-bit Barker code that Wi-Fi LANs use provides insufficient code gain to allow CDMA (code-division multiple access), although high-level protocols implement CSMA (carrier-sense multiple access). The transmitter senses when another transmitter is waiting until the channel is quiet before it can transmit. The 802.11b's bandwidth allows only three and four devices, respectively, to operate at once in those countries that the FCC governs and that European standards govern. If a maximum number of devices are operating, then interference will occur with Bluetooth, WirelessUSB, cordless phones, and ZigBee.

Wireless USB can be a wideband radio at 3-GHz and higher frequencies, but Cypress Semiconductor also has developed a 2.4-GHz WirelessUSB standard. Like Bluetooth, this standard divides the 2.4-GHz band into 79 1-MHz-wide bands, but Cypress uses DSSS rather than FHSS to modulate the signal. The

connection does not hop around the 79 bands but rather sticks to one band. The pertinent thing about this implementation is that it is frequency-agile—that is, if it cannot establish or maintain a good connection in one frequency, it jumps to a different one. WirelessUSB's developers targeted it at replacing cables; it has the low data rates of HID (human-interface devices). The 2.4-GHz ZigBee protocol divides the band into 16 3-MHz-wide channels spaced 5 MHz apart. It uses DSSS to modulate the signal, does not hop among the 16 channels, and does not provide for frequency agility. Cordless phones and baby monitors also use the 2.4-GHz ISM band. Cordless phones may use FHSS or DSSS. They generally divide the 2.4-GHz band into 10 to 20 channels. The phones are rarely agile, but many allow users to select an operating channel to avoid noise.

Figure 6 shows all of these radios and protocols in the 2.4-GHz band. If the spectrum were an ecosystem, you could look at the Wi-Fi wireless LANs like lions at the top of the food chain. They take up a chunk of bandwidth and, when busy, wipe out other traffic in that chunk. Bluetooth devices are like insects flitting about their 79 1-MHz frequency bands. They hop around and pop up at indeterminate times, depending on who is walking by with a headset. If Bluetooth devices are insects, then ZigBee is like a groundhog that pops its head up to see whether spring is near. It takes a wider part of the band but uses it infrequently. Because the groundhog is not agile, its hole is always in the same frequency. Cypress WirelessUSB is like a hyena—an agile hunter that is always prowling around looking for a clear frequency to operate on. Once it finds that frequency, it stays there and can continuously transmit low-data-rate information. The biggest problem in this ecosystem is the cordless phone. Cordless phones are like tigers that can carve through everything. They transmit a powerful signal that drowns out all the other animals in the jungle. For this reason, several Wi-Fi LAN manufacturers recommend that customers do not use cordless phones. The unlicensed, 2.4-GHz band is not unregulated, but the FCC dictates only power levels. The mixture of DSSS- and FHSS-modulation schemes may cause problems for both types of devices.

Two mitigating factors bring light to all this doom: locality and the infrequent transmission of some wireless devices. Even a weak Bluetooth transmitter on your belt will overpower a wireless LAN that is 20 yards away. Engineers at Dust Networks are working to overcome these two drawbacks. Dust doesn't strictly conform to the ZigBee

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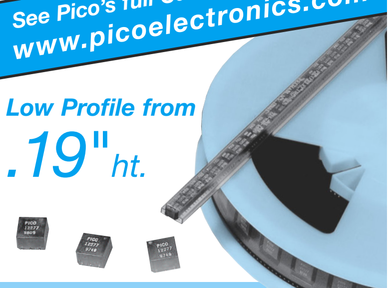

standard because the company provides frequency agility; Dust's devices jump to a different ZigBee frequency to get a clear channel. Texas Instruments has made similar efforts. The company in 2005 bought ZigBee pioneer Chipcon. TI's new ZigBee transmitter has better sensitivity and selectivity than the ZigBee specification to extend radio range and reject any interference. Another approach is simply to use a less populated band. All ZigBee vendors' devices can operate on 800- and 900-MHz bands instead of the crowded 2.4-GHz band. The lower frequency improves range, as well. Zarlink provides the ZL70101 implantable radio chip that uses the 400- to 405-MHz MICS (Medical Implant Communication Service) band. The device provides 800-kbps data rates along with MAC (media-access control) that includes Reed-Solomon-encoding FEC (forward-error-correction) and CRC (cyclic-redundancy-check) error detection and retransmission to achieve a reliable data link.

One innovative company has found a market for building lighting-control products that are simpler than the mesh networks that ZigBee proponents envision. The Lightning Switch by PulseSwitch Systems uses a piezoelectric-powered transmitter to send a code to a 500W ac-line controller using the 434-MHz frequencies that key fobs and garage-door remotes use. The transmitters never need batteries because users supply the energy when they toggle the switch. "Although certain garage-door openers and some remote-car-lock systems are assigned the same frequency by the FCC, there isn't any chance of our transmitters opening someone's garage door or unlocking someone's car," says Jeff Rogers, director of engineering at PulseSwitch. "We use a patented ID-code system formatted to a certain pattern, which is different from that used by car locks and garage-door openers." With more than 268 million codes available, he says, you could have the same number of transmitter-receiver pairs in the same room, and they would not interfere with each other or with other devices working on other ISM frequencies.

Imagine an application in which the DMV (Department of Motor Vehicles) would communicate to your car when it is time for an emissions inspection. The car would then—without human intervention—collect and relay back pollution-performance data over real road loads and drive cycles. You would never need to get another emissions inspection. Nevertheless, look at the long adoption path of Bluetooth; it is now a regular part of most people's lives. As *EDN* Executive Editor Ron Wilson points out, "You can recognize pioneers from the arrows in their backs." The ricochet mobile wireless network was an early wireless-mesh network that failed. The reality of M2M will be neither tragic failure nor wild success but somewhere in the analog middle. And when someone invents that killer application, we will all smack our foreheads and ask, "Why didn't I think of that?" **EDN**

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External components improve SAR-ADC accuracy

DIRECTLY DRIVING THE INPUT OF A CAPACITIVE SAR ADC WITH AN OP-AMP OUTPUT CAN PRODUCE TRANSIENTS THAT DEGRADE THE CONVERTER'S PERFORMANCE. INTERPOSING AN RC NETWORK CAN SOLVE THE PROBLEM–PROVIDED THAT YOU KNOW WHAT VALUES TO USE.

It is tempting to use an op amp to directly drive the input of a SAR (successive-approximation-register) ADC. Unfortunately, this configuration can limit circuit performance. An external RC (resistor-capacitor) network better isolates the converter from the driver amplifier and allows greater flexibility in op-amp selection. Getting the best performance from a SAR ADC may be more important than you think. Even if you convert signals that are well below the frequency limitations of the converter and amplifier, you can't ignore the dynamic characteristics of the SAR ADC's input structure.

Figure 1 shows a single-supply combination SAR-ADC/op-amp circuit. This circuit places the op amp in an inverting-gain configuration. IC_1 is a unity-gain-stable, single-supply CMOS op amp with a gain-bandwidth product of 5 MHz. The single-supply configuration avoids the effect of the amplifier-input limitations, such as a limited input range and input common-mode-crossover distortion. The designer of this circuit uses the ADC-reference output to bias the amplifier's noninverting input as well as the negative input of the ADC, thus keeping the op-amp operation between the supply rails. IC_2 is a 12-bit, 500k-sample/sec SAR ADC.

In **Figure 1**, the circuit appears to be functional; the op amp's low-impedance output drives the SAR ADC. **Figure 2** shows the FFT-test results for this circuit, with a 15-kHz op-amp-input signal. In **Figure 2a**, the SAR ADC's acquisition time equals 265 nsec. In **Figure 2b**, the acquisition time is 560 nsec. These acquisition times extend neither the op amp nor the ADC beyond its specified performance limits.

The measurement results show that the length of the acquisition time affects the performance; increasing the acquisition time from 250 to 560 nsec improves the performance, although increasing the acquisition time also slightly increases the total throughput time. With the longer acquisition time, the SNR (signal-to-noise ratio) increases from 70.8 to 71.5 dB and the THD (total harmonic distortion) decreases from −71.4 to −78.6 dB (**Reference 1**).

STANDARD SAR-ADC MODEL

A capacitive SAR ADC's input stage contains a capacitive-charge-redistribution network (**Figure 3** and **references 2** and **3**). In **Figure 3**, V_{SH0} is the initial voltage across the sampling capacitor, C_{SH}. Depending on the converter's input structure, this voltage can equal the input during the previous conversion, ground, or V_{REF}. Opening S_2 and closing S_1 cause signal acquisition. When S_1 closes, the voltage across the sampling capacitor, C_{SH}, changes to V_{IN}. Charge from the voltage source, V_{IN}, passes through the sampling-switch path of S_1 and R_{S1} onto C_{SH}. As the charge redistributes itself, the charge previously on C_{SH} changes so that V_{CSH} equals V_{IN} (**Figure 4**).

TABLE 1 WORST-CASE SETTLING TIME OF SAR ADC

ADC resolution (bits)	k_1 (time-constant multiplier to 1-LSB accuracy, ½^N)	k_2 (time-constant multiplier to ½-LSB accuracy, ½$^{N+1}$)
8	5.5	6.24
10	6.9	7.62
12	8.3	9.01
14	9.7	10.4
16	11.1	11.78
18	12.5	13.17

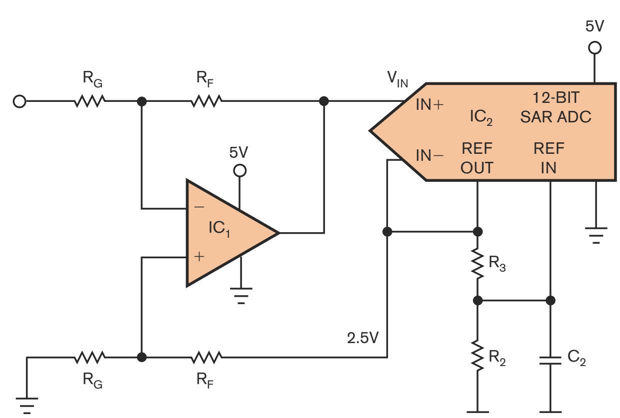


Figure 1 In this sample application circuit for a SAR-ADC system, if $R_F=R_G$, the noise gain for amplifier IC_1 is 2V/V.

If you consider only the ADC input, the ADC's bandwidth depends on the internal sampling capacitor, C_{SH}, and the switch resistance, R_{S1}. From the time constant, $\tau=R_{S1}\times C_{SH}$, you can derive the settling time of this one-pole system. The minimum acquisition time for the SAR converter is the time required for the sampling mechanism to capture the input voltage. The acquisition time begins after the issuance of the sample command and the charging of the hold capacitor, C_{SH}.

You can use the following **equations** to determine the settling time for the network in **Figure 3**.

$$V_{CSH}(t)=V_{CSH}(t_0)+(V_{IN}-V_{CSH}(t_0))\times\left(1-e^{\frac{-t}{\tau}}\right), \quad (1)$$

where $V_{CSH}(t)$ is voltage versus time across the sampling capacitor, C_{SH}; $V_{CSH}(t_0)$ is voltage across the sampling capacitor, C_{SH}, at the start of the acquisition time; V_{IN} is the ADC's input voltage; τ is the acquisition-time constant, equal to $R_{S1}\times C_{SH}$; and t is a time variable in seconds.

If you want the error not to exceed ½ LSB, the time at which the voltage on the sampling capacitor, C_{SH}, approaches within ½ LSB of the input voltage establishes the acquisition time.

$$V_{IN}-V_{CSH}(t_{AQ})\le\frac{1}{2}\text{ LSB}, \quad (2)$$

or

$$V_{CSH}(t_{AQ})\ge V_{IN}-\frac{1}{2}\text{ LSB}, \quad (3)$$

where $V_{CSH}(t_{AQ})$ is voltage across the sampling capacitor, C_{SH}, at the end of the sampling period, and t_{AQ} is the acquisition time, or the amount of time from the beginning of the sampling period (t_0) to the end of the sampling period. Further,

$$\frac{1}{2}\text{ LSB}=\frac{FSR}{2^{N+1}}, \quad (4)$$

where FSR is the input full-scale range of the N-bit converter.

If you change $V_{CSH}(t)$ to $V_{CSH}(t_{AQ})$ and $V_{CSH}(t_0)$ to V_{SH0} and make **equations 1** and **3** equal, you can derive the following **equations**:

$$V_{IN}-\frac{FSR}{2^{N+1}}\le V_{SH0}+(V_{IN}-V_{SH0})\times\left(1-e^{\frac{-t_{AQ}}{\tau}}\right), \quad (5)$$

or

$$t_{AQ}\ge\tau\times\ln\left(\frac{V_{IN}-V_{SH0}}{FSR}\times 2^{N+1}\right). \quad (6)$$

If

$$k=\ln\left(\frac{V_{IN}-V_{SH0}}{FSR}\times 2^{N+1}\right),\quad\text{then} \quad (7)$$

$$t_{AQ}\ge k\times\tau. \quad (8)$$

You can calculate settling time as a function of the input-stage time constant and the time-constant multiplier, k, for a variety of ADC resolutions. **Table 1** summarizes these cal-

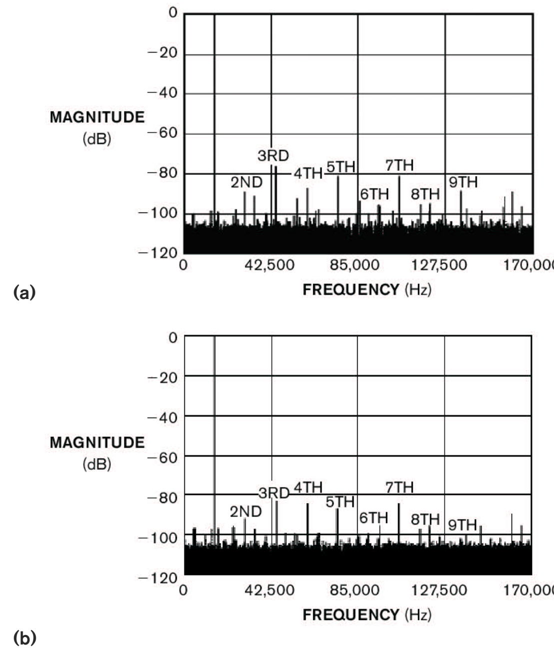


Figure 2 The measured FFT results of Figure 1's 500k-sample/sec, 12-bit SAR ADC show that an acquisition time of 265 nsec produces significant harmonic distortion (a), whereas an acquisition time of 560 nsec decreases harmonic distortion (b).

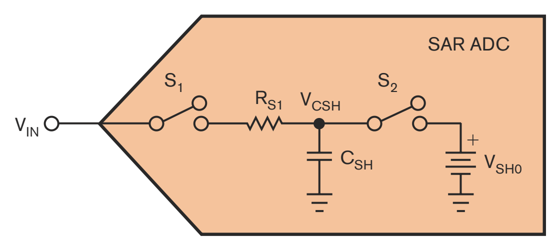


Figure 3 The equivalent input elements for the SAR ADC include an internal input RC pair, R_{S1} and C_{SH}; two switches, S_1 and S_2; and a voltage, V_{SH0}.

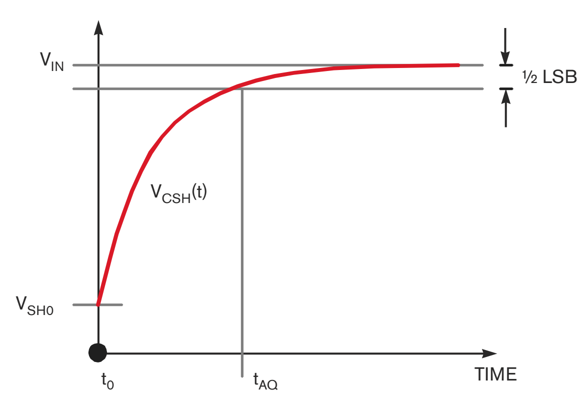


Figure 4 The voltage across the sampling capacitor changes with a single-pole response during the SAR-ADC acquisition period.

culations. You can use these calculations to evaluate the acquisition time of any SAR ADC. For the worst-case analysis (**Equation 5** and **Table 1**), assume that V_{SH0} equals 0V. **Figure 5** shows the change of the initial charge of the Texas Instruments ADS8361, a 16-bit, 500k-sample/sec SAR ADC, as a function of the input-signal amplitude.

With the ADS8361, S_1's closed-switch resistance, R_{S1}, is 20Ω. The ADS8361's internal sampling capacitor, C_{SH}, is equal to 25 pF. From **Figure 5**, you can see that the sinusoidal input voltage frequency is much lower than the converter's sampling frequency. If you measure lower input frequency signals, $f_{IN} \le f_S/10$, the calculation uses an initial voltage on V_{SH0} equal to half of the full-scale range. On the other hand, if there is a front-end multiplexer, V_{SH0} is 0V. For a 16-bit SAR ADC, the time-constant multiplier, k_1, for 1-LSB error equals 11.09. If you need ½-LSB error, $k_2=11.78$. The detailed discussion in **Reference 4** explains how to determine the initial charge of the sampling capacitor in a capacitive SAR ADC.

A CHARGE BANK AT THE SAR-ADC INPUT

Figure 6 illustrates a driving amplifier, followed by an RC pair that connects to the input of a SAR ADC. The capacitor, C_{IN}, acts as a charge bank that supplies ample charge to the SAR ADC's internal capacitor array. Using the previous calculation for a 16-bit SAR ADC, the time constant, τ ($\tau=R_{IN}\times C_{IN}$), of the external RC filter in which $k_2=t_{AQ}/\tau$ is between 11 and 12. A k value of 11 or 12 does not degrade the performance of the signal chain. However, by fine-tuning the formulas, you can achieve optimum performance with lower k values.

EVALUATING THE CHARGE-BANK CIRCUITRY

In the circuit of **Figure 6**, the charge on C_{IN} follows the input voltage before and after the internal ADC sampling switch, S_1, closes. With this condition in mind, the timing evaluation ignores the influence of R_{IN}. **Figure 7** shows the model of a new SAR-ADC system. In this system, capacitors C_{IN} and C_{SH} have different initial voltages. At the start of a conversion, the charge quickly redistributes between C_{IN} and C_{SH} through R_{S1}.

Figure 8 shows a simplified circuit for the capacitive input stage of the circuit in **Figure 7**. Before the input-signal acquisition, S_1 is open (**Figure 8a**). The input capacitor, C_{IN}, has an initial voltage of V_{IN}, and the voltage across the sampling capacitor, C_{SH}, equals V_{SH0}. S_1 closes at the start of signal acquisition (**Figure 8b**). The capacitor voltages, V_{IN} and V_{CSH}, become equal (**Figure 8c**) as the charge quickly redistributes between C_{IN} and C_{SH}.

TABLE 2 CHANGES IN K AS A FUNCTION OF C_{IN}.

ADC resolution (bits)	C_{IN} (pF)	α	k_3 (time-constant multiplier to ½-LSB accuracy)	R_{IN} (Ω)
16	200	8	9.59	1576
16	400	16	8.95	894
16	1000	40	8.07	411
16	4000	160	6.7	126

Notes:
Using worst-case values, V_{IN} is the full-scale voltage, or 2^N, and V_{SH0} is 0V.
$\alpha = C_{IN}/C_{SH}$.

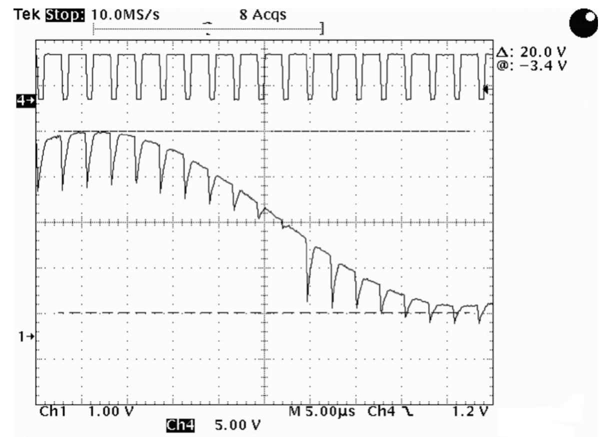


Figure 5 After an acquisition command, the ADS8361 requires a surge of current to charge its sampling capacitor, C_{SH}, for different initial voltages of V_{SH0}.

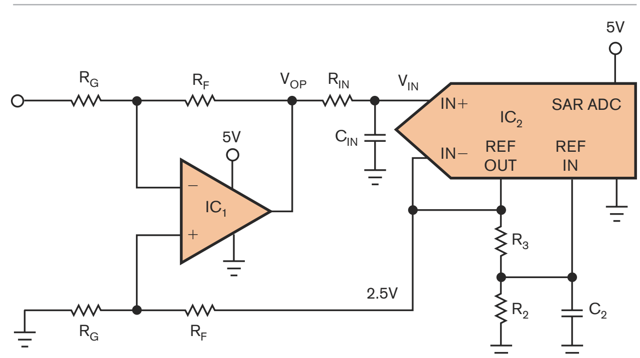


Figure 6 The correct configuration for the external input circuits of the SAR ADC is a driving amplifier followed by an RC network comprising R_{IN} and C_{IN}.

The following **equations** calculate the charge on capacitors C_{IN} and C_{SH}:

$$Q_{IN}=C_{IN}\times V_{IN}, \qquad (9)$$

and

$$Q_{SH}=C_{SH}\times V_{SH0}. \qquad (10)$$

After S_1 closes, the charge on C_{IN} and C_{SH} distributes between the capacitors. C_{IN} and C_{SH} combine into an equivalent capacitance, C_{TOT} (**Figure 8b** and **8c**). The effective capacitance and charge distribution are:

$$C_{TOT}=C_{IN}+C_{SH}, \qquad (11)$$

and

$$Q_{TOT}=Q_{IN}+Q_{SH}. \qquad (12)$$

Using **equations 9** through **12**, you can calculate a new equivalent voltage on capacitors C_{IN} and C_{SH}:

$$V_{TOT} = \frac{C_{IN}}{C_{IN}+C_{SH}} \times V_{IN} + \frac{C_{SH}}{C_{IN}+C_{SH}} \times V_{SH0}. \quad (13)$$

Introducing the ratio $C_{IN}/C_{SH}=\alpha$, **Equation 13** transforms into:

$$V_{TOT} = \frac{\alpha}{\alpha+1} \times V_{IN} + \frac{1}{\alpha+1} \times V_{SH0}. \quad (14)$$

Now, you can calculate the required time constant of the input RC for the circuit in **Figure 6**.

$$V_{TOT}(t) = V_{TOT}(t_0) + (V_{IN} - V_{TOT}(t_0)) \times \left(1 - e^{\frac{-t}{\tau}}\right), \quad (15)$$

where $V_{TOT}(t)$ is the voltage versus time across capacitor C_{TOT} and $V_{TOT}(t_0)$ is the voltage across C_{TOT} at the start of the acquisition time, using **Equation 14**.

Again, to limit the error to ½ LSB, you must make the acquisition time long enough for the voltage on C_{TOT} to approach the input voltage within ½ LSB.

$$V_{IN} - V_{TOT}(t_{AQ}) \le \frac{1}{2}\ \text{LSB}, \quad (16)$$

or

$$V_{TOT}(t_{AQ}) \ge V_{IN} - \frac{1}{2}\ \text{LSB}, \quad (17)$$

where $V_{TOT}(t_0)$ is the voltage across the capacitor, C_{TOT}, at the end of the sampling period. By changing $V_{TOT}(t)$ to $V_{TOT}(t_0)$ and making **equations 15** and **17** equal, you obtain:

$$V_{IN} - \frac{FSR}{2^{N+1}} \le V_{TOT}(t_0) + (V_{IN} - V_{TOT}(t_0)) \times \left(1 - e^{\frac{-t_{AQ}}{\tau}}\right), \quad (18)$$

and

$$t_{AQ} \ge \tau \times \ln\left(\frac{V_{IN} - V_{TOT}(t_0)}{FSR} \times 2^{N+1}\right). \quad (19)$$

Now, you can define a new way of calculating the time-constant multiplier, k_3, using **equations 14** and **19**.

$$k = \ln\left[\frac{\left(1 - \frac{\alpha}{\alpha+1}\right) \times V_{IN} - \frac{1}{\alpha+1} \times V_{SH0}}{FSR} \times 2^{N+1}\right]. \quad (20)$$

Equation 20 shows that k_3 is a function of not only the initial charge, V_{SH0}, but also the external capacitor, C_{IN}. In the ADS8361, a 16-bit SAR ADC with a lower input-frequency signal of $f_{IN} \le f_S/10$, C_{SH}'s calculated initial charge, V_{SH0}, is half of the full-scale range. On the other hand, with the multiplexed signal at the input to the converter, you must use V_{SH0}=0V. With these assumptions, **Equation 20** becomes:

$$k = \ln\left(\frac{1}{\alpha+1} \times 2^{N+1}\right). \quad (21)$$

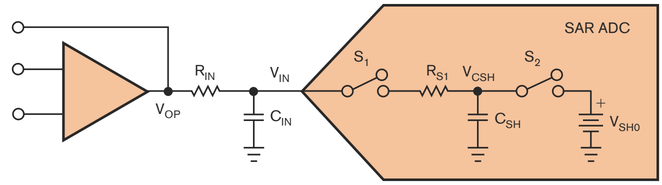


Figure 7 C_{IN}, at the SAR-ADC input, provides a charge reservoir during sampling.

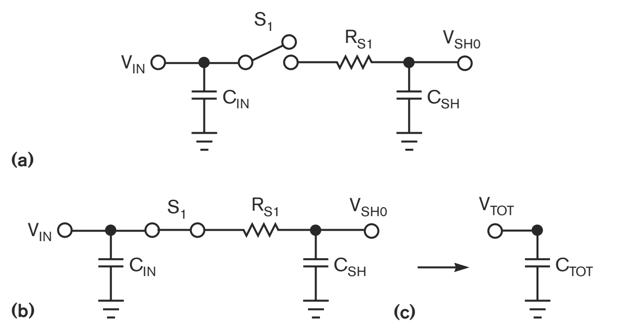
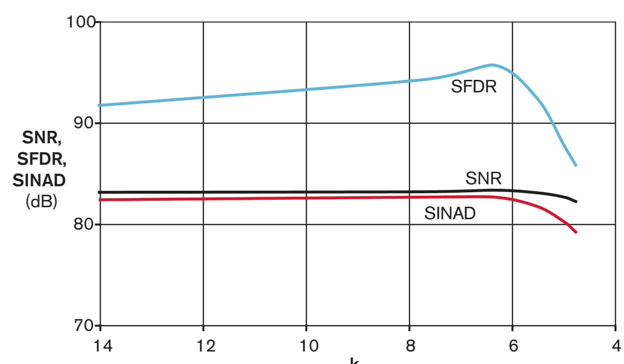


Figure 8 These simplified models describe the external and internal ADC capacitors.



NOTES: CLOCK=9.9968 MHz.
SAMPLING FREQUENCY=199.936 kHz.
INPUT-SIGNAL FREQUENCY=9982.15625 Hz.
ACQUISITION TIME=3.4 μSEC.

Figure 9 Results measured from the circuit of Figure 6 show that acquisition time has little effect on SNR and SINAD until you reduce the time-constant multiplier, k, to less than 6. SFDR reaches a maximum when k is slightly greater than 6. The circuit's active devices are Texas Instruments' 16-bit ADS8361 ADC and OPA350 single-supply CMOS amplifier.

Table 2 shows how k_3 changes as a function of C_{IN} and shows lower valued time-constant multipliers, k_3, for **Figure 6**'s 16-bit SAR ADC.

TEST RESULTS

Figure 9 shows the results for the ADS8361, a 16-bit converter, tested in the configuration in **Figure 6**. The results show that the ADS8361 maintains good performance with

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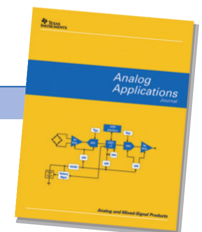
BRIEF

Enhanced-Safety, Linear Li-Ion Battery Charger with Thermal Regulation and Input Overvoltage Protection

By Jinrong Qian

Applications Manager, Battery Management Applications

The lithium-ion (Li-ion) battery is widely adopted in portable devices because of its high energy density on both a gravimetric and volumetric basis. Due to their simplicity, low cost, and small size, highly integrated linear battery chargers are widely used to charge single-cell Li-ion batteries. However, when unregulated adapters are used to power portable systems, it can be a challenge to remove or minimize the heat generated from the linear chargers and to maintain their operation within a safe thermal range. This article describes a newly developed battery charger with thermal regulation. This charger has input overvoltage protection (OVP), which alleviates thermal concerns while maximizing the charge rate and minimizing the charging time, allowing use of an unregulated adapter.



Battery-Charging Requirements

The charge profile widely used for charging Li-ion batteries consists of three charging phases: precharge; fast-charge constant current (CC); and constant voltage (CV). In the precharge phase, the battery is charged at a low rate when the cell voltage is below 3.0 V. Typically, when the cell voltage reaches 3.0 V, the charger enters the CC phase. The faster-charge CC is usually limited to stay below the cell's 1C rating. The cell cycle life decreases with charge rates above 1C because metallic lithium deposited on the node easily reacts with the electrolyte and is permanently lost. Finally, the charger enters the CV phase, where it maintains the peak cell voltage and then terminates charging when the charge current drops to a predefined level.

The cell capacity is a function of the cell voltage—the higher the voltage, the higher the capacity. However, higher cell voltage results in shorter cycle life. For example, charging a cell at 4.3 V can provide 10% more capacity, but cell cycle life may be 50% shorter. On the other hand, if the cell is undercharged at just 40 mV under the optimum voltage, it can have about 8% lower capacity. Therefore, a very accurate battery charge voltage is extremely important.

Thermal-Regulated Battery Charger with Input OVP

Figure 1 shows a low-cost, stand-alone linear battery charger circuit with thermal regulation and input OVP. The charger simply drops the adapter's DC voltage down to the battery voltage. The power dissipation in the linear charger is given by

$$P_{CHGR} = (V_{IN} - V_{BAT}) \times I_{CHG}.$$

There is a large difference between the input and battery voltages when the charger transitions from precharge to fast-charge mode, where the power dissipation reaches the maximum. For example, if a 5-V adapter is used to charge a 1200-mAh Li-ion battery, it has a maximum power dissipation of 1.8 W with a 1-A charge current and a 3.2-V battery voltage. This power dissipation results in an 85°C temperature rise for a 3 x 3-mm QFN package with 47°C/W thermal impedance. The junction temperature exceeds the maximum allowed operating temperature of 125°C at 45°C

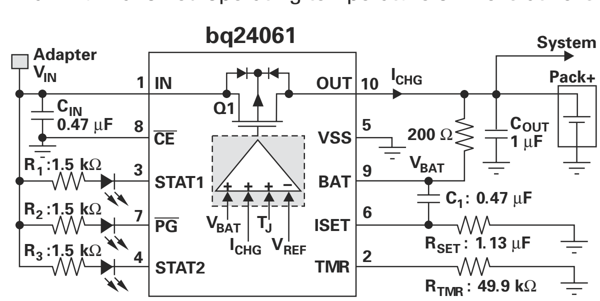


Figure 1: Charger with thermal regulation and input OVP

ambient temperature. It is hard to maintain the junction temperature within a safe thermal range at the beginning of the charging. As the battery voltage rises during the charging, the power dissipation drops. After charging enters the CV mode, the power dissipation drops further as the charge current starts to taper down.

How do we improve the design to keep the charger operating in a safe thermal range? The more advanced battery chargers such as bq2406x and bq2403x have introduced a thermal regulation loop to prevent overheating of the charger. When the internal chip temperature reaches a predefined temperature threshold—for example, 110°C—any further increase of the IC temperature results in reduction of the charge current. This limits the power dissipation and provides thermal protection to the charger. The maximum power dissipation causing the IC junction temperature to reach thermal regulation depends upon the PCB layout, the number of thermal vias, and the ambient temperature. Figure 2 shows that after 1.2 seconds the thermal loop reduces the effective charging current from 1.2 A to 600 mA within 2 seconds.

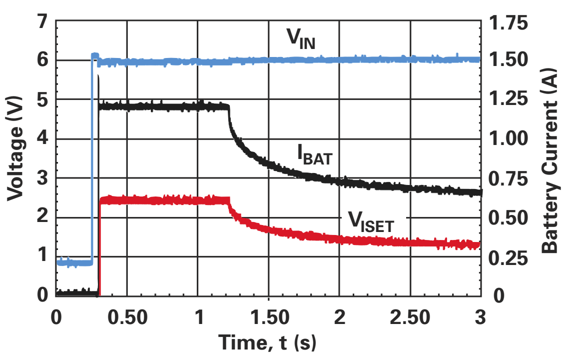


Figure 2. Charge-current with thermal regulation

Thermal regulation usually happens at the early stage of the fast charge, but if it is active during the CV mode, the charging current could prematurely reach the charge termination threshold. To prevent this false charge termination, the battery charge-termination function is disabled whenever the thermal regulation loop is active. In addition, the effective charge current is reduced, which increases the battery charging time and which, if the charge safety timer had a fixed setting, could terminate charging early. The bq2406x employs a dynamic safety-timer control circuit that effectively extends the safety time during thermal regulation and minimizes the chance of a safety-timer fault. Figure 3 shows that the safety-timer response is inversely proportional to the effective charge current in thermal-regulation mode.

When the battery-charging function is enabled, the internal circuit generates a current proportional to the real charging current set by the ISET pin. The voltage generated across resistor R_{SET} reflects the charge current. This voltage can be monitored by the host for charge-current information.

There are several types of adapters used to charge Li-ion batteries. Less expensive adapters may not have well regulated output and have higher output voltages under no load than at the normal load. In addition, during the battery

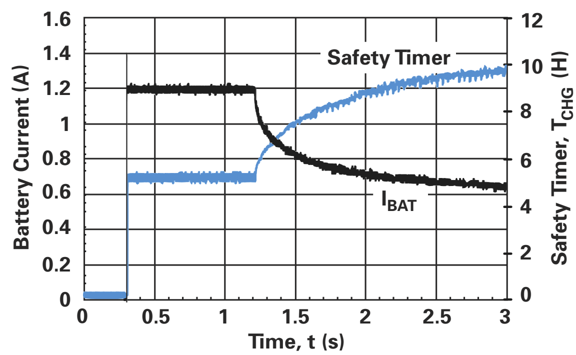


Figure 3. Dynamic safety timer in thermal regulation

hot plug-in, the input voltage to the charger could reach as high as two times that of the adapter voltage due to resonance between the cable inductance and the input capacitor of the battery charger. To increase safety when the input voltage is above the predefined threshold, the input OVP implemented in bq2406x chargers does not allow charging.

Many applications require powering the system while charging the battery simultaneously. When the system is directly connected to the battery-charge output as shown in Figure 1, interaction between the system and charger may result in a false charge termination caused by the safety timer. Figure 4 shows a typical application circuit that eliminates such issues. There are two independent power paths, one to charge the battery and one to power the system. When the AC adapter is not available, the battery discharge MOSFET is turned on after a time delay set by R_4 and C_2 so that the battery will provide power to the system.

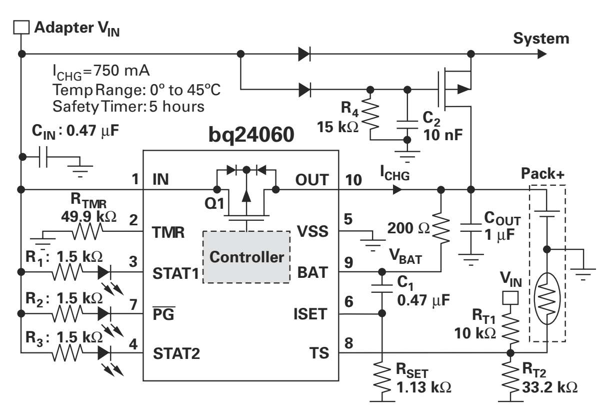


Figure 4. Power-path-management battery charger

Summary

The linear battery charger with thermal regulation can significantly improve the thermal design and safety. With input OVP, it allows only authorized adapters to charge the battery, improving system safety.

References:

1. bq2406x Datasheet (SLUS689A)
2. *power.ti.com*

SNR, SFDR (spurious-free dynamic range), and SINAD (signal, noise, and distortion) until k_3 becomes smaller than six. This result differs from the k_1-multiplier values of 11.1 and 11.78 that **Table 1** generates. In **Figure 9**, the 16-bit ADS8361 SAR ADC operates at 200k samples/sec (t_{AQ}=3.4 µsec). The frequency of the input signal is 10 kHz. In **Equation 20**, the initial voltage on V_{SH0} is equal to half the full-scale range. The value of the sampling capacitor, C_{SH}, is 25 pF, and the value of C_{IN} is 2.2 nF. With these assumptions, **Equation 20** becomes:

$$\alpha = \frac{C_{IN}}{C_{SH}} = \frac{2.2\text{ nF}}{25\text{ pF}} = 88, \qquad (22)$$

$$\begin{aligned} k_4 &= \ln\left[\frac{\left(1-\frac{\alpha}{\alpha+1}\right)\times V_{IN}-\frac{1}{\alpha+1}\times V_{SH0}}{FSR}\times 2^{N+1}\right] \\ &= \ln\left[\frac{\left(1-\frac{88}{88+1}\right)\times 5V-\frac{1}{88+1}\times 2.5V}{5V}\times 2^{16+1}\right] = \end{aligned} \qquad (23)$$

and

$$\begin{aligned} R_{IN} &= \frac{t_{AQ}}{k_4\times(C_{IN}+C_{SH})} \\ &= \frac{3.4\ \mu\text{SEC}}{6.6\times(2.2\text{ nF}+25\text{ pF})} = 231.5\Omega. \end{aligned} \qquad (24)$$

Note that, in **Figure 9**, the improvement in SFDR is approximately 5 dB.

A LITTLE RC FINESSE HELPS

The following **equations** illustrate the key design guidelines for the SAR-ADC input circuits in **Figure 6.**

$$\tau = R_{IN}\times(C_{IN}+C_{SH}) \le \frac{t_{AQ}}{k}. \qquad (25)$$

For multiplexed signals, this **equation** is:

$$k = \ln\left(\frac{1}{\alpha+1}\times 2^{N+1}\right). \qquad (26)$$

And, for lower-input-frequency signals,

$$k = \ln\left[\frac{\left(1-\frac{\alpha}{\alpha+1}\right)\times V_{IN}-\frac{1}{\alpha+1}\times V_{SH0}}{FSR}\times 2^{N+1}\right], \qquad (27)$$

where $\alpha = C_{IN}/C_{SH}$.

To maximize the system's SNR, the value of C_{IN} should be as large as possible with the op amp's driving capability in mind. For preservation of the ADC's THD, C_{IN} should be either a ceramic device with a chip-on-glass dielectric or a silver-mica

unit with ≤5% tolerance. The value of R_{IN} depends primarily on the acquisition time, the value of C_{IN}, and the op amp's driving capability. R_{IN} isolates amplifier IC_1 from load capacitor C_{IN}, which, for low-noise performance, should be a metal-film device with ≤1% tolerance. The RC filter between the op amp and the SAR ADC may compromise the amplifier's stability. **Reference 5** provides more details on op-amp selection and stability. EDN

ACKNOWLEDGMENT

The authors wish to express special thanks to Art Kay, a senior applications engineer for Texas Instruments, for his help in developing the concept discussed herein.

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AUTHORS' BIOGRAPHIES

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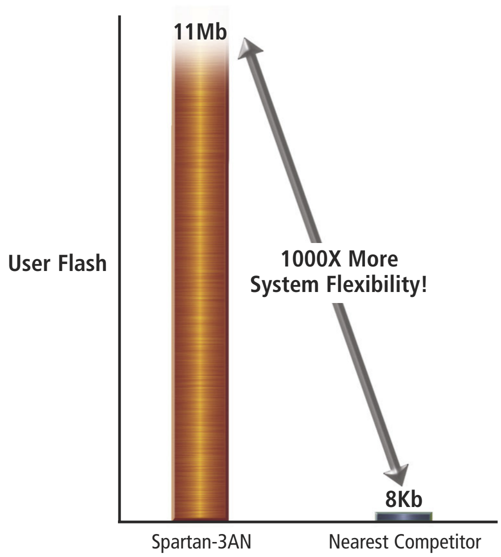

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Digital-debugging methods save time

THREE LOGIC-ANALYZER TECHNIQUES COMBINE STIMULUS AND REAL-TIME CAPTURE FOR CIRCUIT VALIDATION AND DEBUGGING.

If you are performing validation tests or debugging circuits, you can save time by using three logic-analyzer techniques that combine stimulus and real-time trace capture: simulating the input to a circuit and capturing traces with the logic analyzer to validate the correct response to a given stimulus; using the logic analyzer to capture traffic and quickly convert the real-time trace into a stimulus for a pattern generator; and introducing known input errors, using the pattern generator, to test the circuits' reaction to inputs that are out of specification.

The first technique involves a classic method for testing the function of a circuit. A pattern generator simulates the input to a circuit, and a logic analyzer captures traces to validate that the circuit provides the correct response to the given stimulus. A logic analyzer with a built-in pattern generator provides an integrated approach to digital-system validation and debugging. This technique is particularly useful if design teams are working in parallel and the input component is unavailable. If the engineers designing Subsystem B are ready to test before subsystems A and C are ready for test, a pattern generator can provide the inputs to Subsystem B while a logic analyzer observes the outputs of Subsystem B (**Figure 1**). Using this technique, it is theoretically possible to test every possible combination of inputs and observe the corresponding outputs.

On smaller systems, you can map all the possible inputs with corresponding outputs and then test each one. Because of time and resource constraints, engineers who are designing complex systems typically test operational limits or worst-case combinations, sometimes referred to as "corner cases." An example of a worst-case test for high-speed digital tests is to provide stimulus that alternates the inputs at the fastest data rate specified for the circuit. You would then check for functional errors at the output with a logic analyzer. Common test patterns include alternating hex values A and 5 on a bus or "walking ones." The walking-ones pattern individually tests each bit on a bus. Start by holding the least-significant bit on a bus high. Hold all other bits low. On each clock cycle, the high value moves to the next higher bit on the bus.

An example of a worst-case test for transmission lines, buffers, or other circuits that pass signals through unaltered is to test for corrupt data from crosstalk by holding one signal, the victim, either high or low while providing alternating ones and zeros patterns on signals, or aggressors, close to the victim signal. For worst-case situations, all of the bits except one on a bus are aggressors. To perform this testing, configure the pattern generator to run repetitively at the input to a transmission line, the driver of a circuit, to check circuit performance, and note whether the receiving end of the circuit sees any errors. Alternatively, you can have the logic analyzer trigger if the victim signal ever changes at the receiver. To view crosstalk on a victim signal, use an oscilloscope or a logic-analyzer system that can capture eye diagrams (**Figure 2**). In the **figure**, simultaneously alternating patterns on the rising edge of a 180-MHz clock drive seven aggressor signals. The victim trace is one of the center traces of an 8-bit bus routed through an FPGA on a small PCB (printed-circuit board). Comparing the size of the victim signal, the **figure** shows that the crosstalk is approximately 20% of the TTL (0 to 5V)-voltage swing of the aggressor signals.

A worst-case test for ISI (intersymbol interference) checks for when any line has insufficient time to charge to a high level or discharge to a low level because of a weak driver or inappropriate termination. You can use the pattern generator to inject patterns that provide worst-case situations for ISI. On any one signal, alternating 12 high states (ones), followed by one low (zero) state, followed by 12 more high states (11111 1111111011111111111110 ...) is one pattern useful for uncovering potential ISI on individual lines. You can also use the inverse pattern (0000000000001000000 ...). These patterns let the signal achieve maximum or minimum charge and then attempt to perform one pulse in the opposite direction. Insufficient drive strength can result in the signal swing's failure to attain necessary voltage levels at the receiving end of the transmission line during the single pulse.

Healthy systems have no problem handling stressful bit pat-

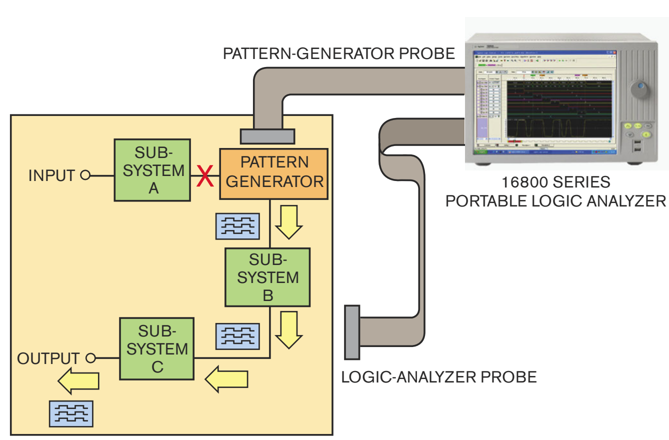

Figure 1 You insert the pattern generator as the input to Subsystem B with the path from Subsystem A disconnected. The logic analyzer captures the response at the output of Subsystem B or Subsystem C as the signals progress through the system.

terns. When you are debugging system problems and intermittent problems are difficult to pinpoint, you can simulate the inputs while observing the outputs to divide and conquer. The combination of subdividing a system for debugging and using a pattern generator to provide a stimulus to an isolated circuit is one way to eliminate suspect circuits in a faulty system. For additional insight into parametric issues on unhealthy systems, you can use an oscilloscope to view analog signals that are time-correlated to the functional trace from the logic analyzer (**Figure 3**).

CAPTURE DRIVING STIMULUS

Using a logic analyzer to capture traffic and quickly convert the real-time trace into test vectors for a pattern generator can greatly simplify the task of writing test vectors for the pattern generator. Test vectors determine the pattern output at each clock cycle. Test vectors are positioned in a list called a sequence. When a sequence runs, the list of vectors executes in order, first vector to last vector. Software tools are available to automatically convert pattern-generator vectors directly from captured logic-analyzer traces (**Figure 4**).

Alternatively, using a manual cut-and-paste process from a logic-analyzer CSV (comma-separated-value) file into a pattern-generator CSV file is relatively easy. If you choose this method, remember that, in every pattern-generator application, you have two sequences. The initialization sequence places your circuit or subsystem in a known state. The main sequence follows the initialization sequence, and you use it for the actual pattern generation that stimulates your circuit under test. The initialization sequence executes only once, and the main sequence loops for repetitive execution. By setting up your pattern generator with the labels and clock settings for your system and then saving a pattern-generator CSV file, you will have the correct initialization sequence in the pattern-generator CSV file. Simply cut and paste the data from the same label names in the logic-analyzer CSV file into the main sequence of the pattern-generator CSV file to copy the trace information.

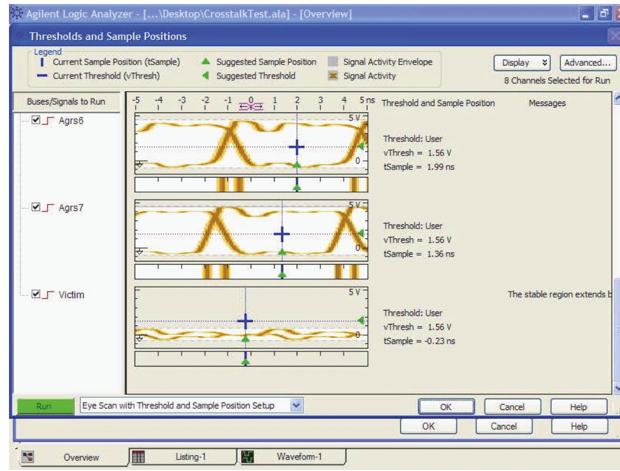

Figure 2 A logic analyzer can provide eye diagrams to compare the level of crosstalk on a victim trace with normal signal swing.

You can modify trace conversions in the pattern generator to alter the stimulus in subtle or pronounced ways. Consider a new design that will increase the data rate of a design from 50 to 100 MHz. To provide stimulus to the new design, you can convert a trace from input to the old system into a pattern-generator trace. You then set the pattern-generator clock to 100 MHz using an internal or an external clock. Use an internal-clock source when you want to have control over the frequency of the output vectors and when it is not important for the output vectors to synchronize to the system under test. Use an external clock if you need to synchronize the vector output of the pattern generator to the system under test.

If capturing a trace to convert into a file is not an option in your design, the pattern-generator interface allows for direct input or loading ASCII text, CSV, or XML files. For complex designs, consider SynaptiCAD's (www.syncad.com) WaveFormer Pro timing-diagram editor and waveform-conversion tool. WaveFormer Pro can generate pattern-generator files from simulation waveform data that SPICE, VHDL, and Ver-

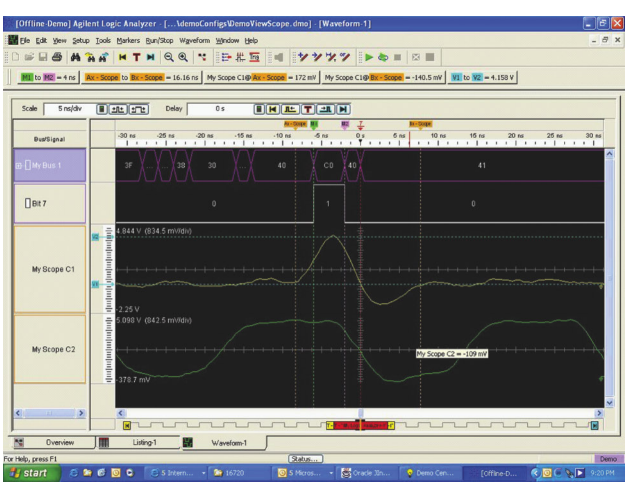

Figure 3 Tools such as ViewScope can pull an oscilloscope trace into the display so the analog characteristics of the signal are time-correlated to the functional trace from the logic analyzer.

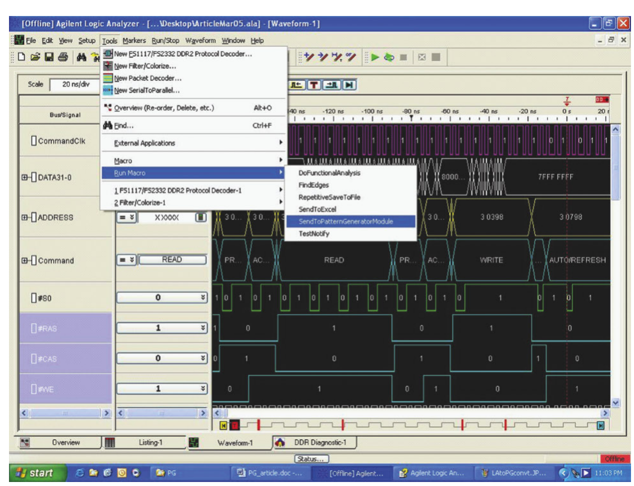

Figure 4 The tool's pulldown menu operating with Agilent 16900 or 16800 Series logic-analysis systems supports converting a trace to a pattern-generator input.

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ilog simulators produce. It can import and export more than 33 files to and from more than 33 simulators and test-equipment platforms. WaveFormer Pro can also read logic-analyzer files and generate VHDL and Verilog testbench modules, as well as SPICE piecewise-linear-voltage-source code.

When you write code for the pattern generator, you can include predefined instruction elements in both initialization and main sequences. Instructions can create breaks and loops, wait for external events or arm, or send an arm signal to another instrument. The user-defined macro lets you create reusable sequences that accept parameters. This flexibility is useful in prototype turn-on and environmental testing.

INJECT ERRORS

With the third technique, consider the fact that the pattern generator is not limited to producing perfect data. Many engineers use their pattern generators to validate the output of their circuits under a variety of inputs that push the limits of the circuit under test. You can purposely introduce errors to test protocol-checking software, interrupt handling, or error-handling software. Examples of error-checking tests include alternating the input data rates faster than specified for the circuit; injecting protocol violations, such as writing to a bank that has not been activated in a DDR-memory circuit; and injecting an interrupt into a circuit and observing the response.

The exact output pattern, clock type and speed, and number of required signals depend on your application. How you configure the pattern generator and the kind of signal-generation sequence you create will vary. However, from a procedural standpoint, the steps are the same each time to set up, create a sequence, and start the pattern generator:

1. Select the probing that is compatible with your device under test.
2. Set the output mode and the clock-source parameters.
3. Connect the probes to your circuit and define buses and signals in the pattern-generator user interface.
4. Create a sequence of test vectors to generate the desired output signals.
5. Run the pattern generator and measure the device under test for the desired results.

Combining a pattern generator with a logic analyzer offers digital-system designers a flexible platform for stimulus and response testing and debugging techniques. Designers use pattern generators to emulate digital signals in circuits under development. The pattern generator can take the place of missing devices, or it can act as a stimulus to functionally test prototypes. **EDN**

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Jennie Grosslight graduated from the University of Colorado (Colorado Springs) with a bachelor's degree in electrical engineering. She has 17 years of experience at Agilent Technologies in system engineering, high-speed-hardware design and validation, product marketing, application support, and project management.

Simple fixture determines leakage of capacitors and semiconductor switches

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

The circuit in **Figure 1a** comprises a voltage follower, IC_1, and the reference-voltage source of IC_2. IC_1 is an Analog Devices (www.analog.com) AD8661 op amp, which has a guaranteed input-bias current of no more than 1 pA and a typical input-bias current of 0.3 pA (**Reference 1**), and IC_2 is an Analog Devices ADR391 precision voltage reference (**Reference 2**). The manufacturer trims the input offset voltage of this op amp not to exceed 100 μV, and the typical value is 30 μV. These properties suit this amplifier for observing self-discharging of almost any type of capacitor. The leakage currents of solid-tantalum capacitors and those having high-quality plastic dielectrics are well above the input-bias current of voltage follower IC_1. The CUT (capacitor under test) initially charges to the reference-voltage level of 2.5V by connecting Point A to the output of IC_2. Subsequently, at some convenient time, Point A disconnects from the source of the reference voltage. A DVM (digital voltmeter) measures the output voltage of the follower at some reasonable time. The measured voltage drop, V_O, with regard to initial value, should be 0.1 to 0.5V. The leakage current, I_O, is $C\times\Delta V_O/t_{MEAS}$, where C is the value of the CUT and t_{MEAS} is the time between releasing the connection of the CUT to the 2.5V source and the instant of readout at the voltage drop of V_O.

The fixture also allows determining leakage currents of reverse-polarized diodes and of various switching devices in the off state, such as JFETs, MOSFETs, BJTs (bipolar-junction transistors), SCRs (silicon-controlled rectifiers), and IGBTs (insulated-gate bipolar transistors). In this case, the parallel combination of the DUT (device under test) and the added capacitor, C_{ADD}, replaces the CUT (**Figure 1b**). The measurement and the formula for evaluating the value of leakage current are the same as those for leakage current in the **equation** $I_O=C\times\Delta V_O/t_{MEAS}$, but C_{ADD} substitutes for the CUT. A polystyrene-dielectric, 10-nF C_{ADD} works well for low-power devices. For high-power devices, however,

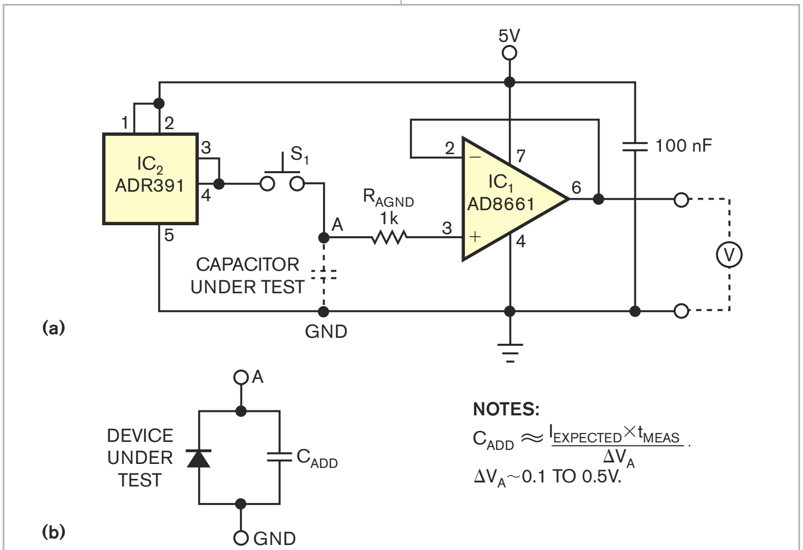

Figure 1 This simple fixture first impresses a reference voltage across a capacitor under test and then measures the voltage drop versus time at the output of the voltage follower (a). The circuit measures the leakage current of a reverse-biased active device (b).

DIs Inside

the value of C_{ADD} should be at least 10 times the value of the parasitic capacitance of the DUT at 0V.

Further, the fixture in **Figure 1b** can also determine the values of resistors of tens of megohms to about 2 TΩ. The current in the **equation** $I_O = C \times \Delta V_O / t_{MEAS}$, in this case, is the current flowing through resistor R_{AGND} at approximately the reference voltage. The resistance is roughly:

$$R_{AGND} \approx V_{REF} \times \frac{t_{MEAS}}{C_{ADD} \times \Delta V_O},$$

or, more precisely:

$$R_{AGND} = \left(\frac{V_{REF}}{\Delta V_O} - \frac{1}{2} \right) \frac{t_{MEAS}}{C_{ADD}}.$$

In all measurements, the voltage drop of V_O should not exceed about one-fifth of the reference-voltage value to allow approximating the inherently exponential droop of V_O by a linear decrease. The pushbutton switch in **Figure 1a**, S_1, must exhibit a leakage of less than 1 pA. Stranded, isolated leads terminated with a gold-plated phosphorus-bronze pin can serve as a low-leakage switch. You can find gold-plated metal pieces in any type of high-quality connectors. Also, you can clip the DUT or CUT between two gold-plated clips made of similar connector parts. To minimize the circuit's leakage, it uses no PCB (printed-circuit board).**EDN**

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1. AD8661 16V Low Cost, High Performance CMOS Rail-to-Rail Operational Amplifiers, www.analog.com/en/prod/0,2877,AD8661,00.html.
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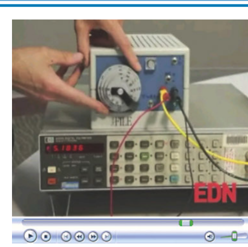
Recycle precision potentiometers as useful voltage sources

Mark Thoren, Linear Technology, Milpitas, CA

An analog- or a mixed-signal lab cannot have too many voltage sources. A simple, reasonably high-precision voltage source can set bias points in an op-amp circuit, tweak the feedback node of a power supply through a large resistor, or run a quick linearity test on an ADC. Engineers often use a dc-power supply because it is the only thing they can find, and many labs lack a true voltage-calibration source. This Design Idea describes a circuit that recycles old precision potentiometers that have direct-reading scales into useful laboratory "volt boxes."

Several types of potentiometers work in the circuit in **Figure 1**. Standard 10-turn potentiometers typically have 0.1% linearity and work well for general-purpose tweaking. However, a five-decade Kelvin-Varley divider with a total resistance of 100 kΩ or less achieves 10-ppm accuracy. Having some indication from a voltage source that its output is correct proves useful. A digital panel meter is one way of achieving this goal. However, even a 0.1% potentiometer is more accurate than most of these meters. So, to indicate that the output is correct, you need to know only whether the power is on, whether the supply voltage is high enough, and whether the output amplifier is working properly and not sourcing or sinking too much current or oscillating.

EDN tech clips



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A single red-green-blue LED provides all three indications. The green LED flashes at a low duty cycle when the power is on and stays lit continuously when the battery voltage is too low. The red LED illuminates when the output is out of regulation because IC_{4B} is a low-duty-cycle relaxation oscillator that pulses a green LED for 5 msec at approximately 0.5 Hz. The blue LED lights when sinking too much current. If the output is oscillating, the LED glows purple.

IC_{4A} compares the positive battery voltage to the precision 10V reference output and continuously turns on the green LED when the positive battery voltage drops below 11.5V. This level is the dropout voltage of the reference, so you know it's time to change the batteries. The load on the positive supply is greater than that on the negative supply, so these cells wear out first. And, because only two cells constitute the negative supply, battery wastage is minimal. Alternatively, you can move the negative cells to the positive side to squeeze the last bit of juice from them.

The reference is IC_1, an LT1236-10 with an added trim circuit. The LT1236 is quiet and stable over time and temperature. Its output drives the top of the precision potentiometer or Kelvin-Varley divider. The output of the circuit is trimmed to 10V when the potentiometer or divider is at its maximum value. The two halves of an LT1881 amplifier, IC_{2A} and IC_{2B}, buffer the output of the potentiometer or divider. The combined bias current for both buffers is 400 pA maximum, which causes a change of approximately 10 μV in the output voltage of a 100-kΩ potentiometer when it is at midscale. Make sure to properly guard the noninverting inputs to prevent leakage. The 50-μV maximum offset and 130-dB CMRR (common-mode-rejection ratio) keep overall accuracy well within 10 ppm of a 10V total span.

One-half of the LT1881 is the voltage output of the volt box. The other half is necessary to drive the two inputs to IC_5, an LT1017 dual comparator that has an input-bias current of 15 nA per comparator. Q_1 to Q_6 form a 100-μA current sink and source referred to the negative supply and positive supply, respectively. You adjust potentiometers R_1 and R_2 to set up a window around the output voltage that is compared with the output of IC_{2A}, which is a replica of the correct output voltage. If IC_{2B} is sourcing or sinking too much current, one of the comparators will trip, turning on the respective LED. If the output is oscillating, both LEDs will light. The window is adjustable from 0 to approximately ±9.3 mV; ±1 mV is a good place to start.

Should you need more output current than the 5 mA that the LT1881 guarantees, you can switch in an LT1010 buffer to provide a "turbo-boost" feature, increasing the output-current capability to ±150 mA and greatly increasing the ability to drive capacitive loads. You should normally disable this buffer because it draws 10 mA more from the supply. Switch S_3 allows reverse polarity, and, if you use a center-off switch, you can disconnect the output. S_1 is the power switch and can also select power from an external supply or battery power when isolation is critical. EDN

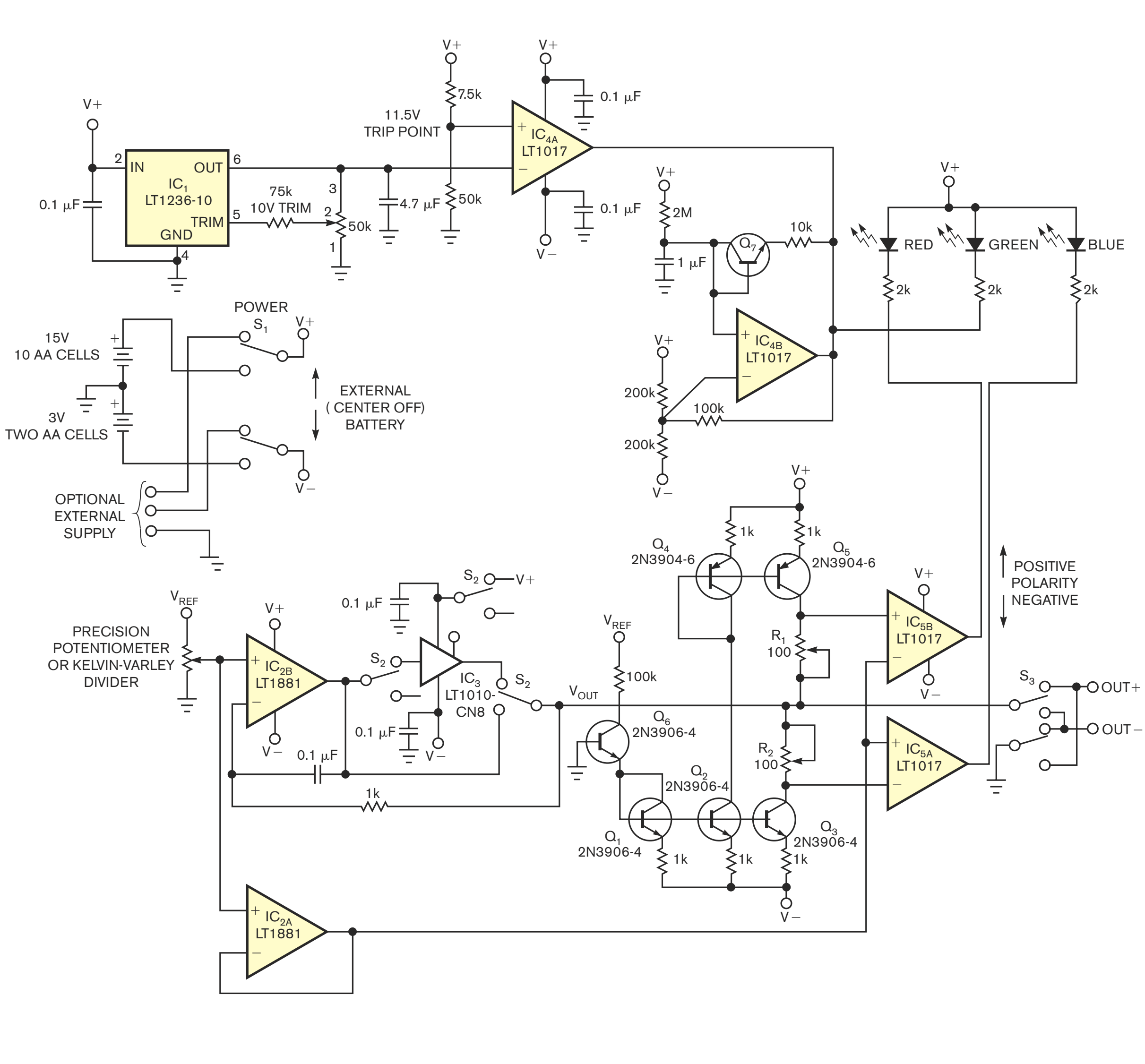

Figure 1 You can recycle old 10-turn potentiometers as precision "volt boxes." The LEDs provide a visual indication that the output voltage is in regulation.

Circuit breaker provides overcurrent and precise overvoltage protection

Anthony H Smith, Scitech, Bedfordshire, England

Requiring only a handful of inexpensive components, the circuit breaker in **Figure 1** responds to both overcurrent- and overvoltage-fault conditions. At the heart of the circuit, D_2, an adjustable, precision, shunt-voltage regulator, provides a voltage reference, comparator, and open-collector output, all integrated into a three-pin package.

Figure 2 shows a simplified view of the ZR431, D_1. The voltage appearing at the reference input is compared with the internal voltage reference, V_{REF}, nominally 2.5V. In the off state, when the reference voltage is 0V, the output transistor is off, and the cathode current is less than 0.1 μA. As the reference voltage approaches V_{REF}, the cathode current increases slightly; when the reference voltage exceeds the 2.5V threshold, the device fully switches on, and the cathode voltage falls to approximately 2V. In this condition, the impedance between the cathode and the supply voltage determines the cathode current; the cathode current can range from 50 μA to 100 mA.

Under normal operating conditions, D_2's output transistor is off, and the gate of P-channel MOSFET Q_4 goes through R_9, such that the MOSFET is fully enhanced, allowing the load current, I_{LOAD}, to flow from the supply voltage, $-V_S$, through R_6 into the load. Q_2 and current-sense resistor R_6 monitor the magnitude of I_{LOAD}, where Q_2's base-emitter voltage, V_{BE}, is $I_{LOAD} \times R_6$. For normal values of I_{LOAD}, V_{BE} is less than the 0.6V necessary to bias Q_2 on, such that the transistor has no effect on the voltage at the junction of R_3 and R_4. Because the input current at D_2's reference input is less than 1 μA, negligible voltage drops across R_5, and the reference voltage is effectively equal to the voltage on R_4.

In the event of an overload when I_{LOAD} exceeds its maximum permissible value, the increase in voltage across R_6 results in sufficient base-emitter voltage to turn on Q_2. The voltage on R_4 and, hence, the reference voltage now pull up toward V_S, causing D_2's cathode voltage to fall to approximately 2V. D_2's output transistor now sinks current through R_7 and R_8, thus biasing Q_3 on. Q_4's gate voltage now effectively clamps to the supply voltage through Q_3, and the MOSFET turns off. At the same instant, Q_3 sources current into R_4 through D_1, thereby pulling the voltage on R_4 to a diode drop below the supply voltage. Consequently, no load current flows through R_6 because Q_2, whose base-emitter voltage is now 0V, has turned off. As a result, no load current flows through R_6, D_2's output transistor latches on, and the circuit remains in its tripped state in which the load current is 0A. When choosing a value for R_6, ensure that Q_2's base-emitter voltage is less than approximately 0.5V at the maximum permissible value of the load current.

As well as responding to overcurrent conditions, the circuit breaker also reacts to an abnormally large value of the supply voltage. When the load current lies within its normal range and Q_2 is off, the magnitude of the supply voltage and the values of R_3 and R_4, which form a potential divider across the supply rails, determine the voltage at the reference input. In the event of an overvoltage at the supply voltage, the voltage on R_4 exceeds the 2.5V reference level, and D_2's output transistor turns on. Once again, Q_3 turns

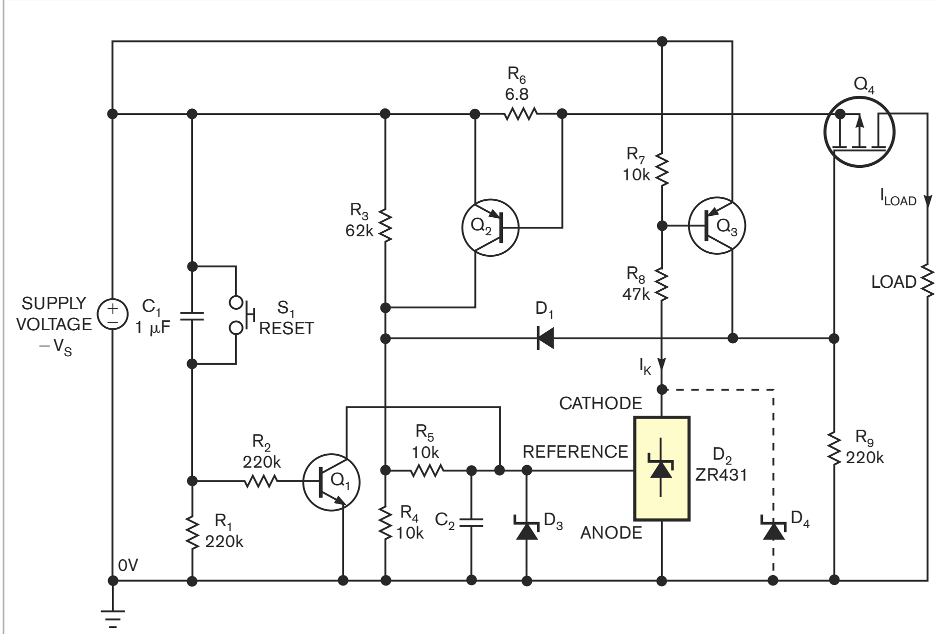

Figure 1 This circuit breaker provides both overvoltage and overcurrent protection. Other than the current flowing in R_3, R_4, and D_2's cathode, the circuit draws no current from the supply in its normal untripped state.

LINEAR TECHNOLOGY

DESIGN NOTES

Direct Efficient DC/DC Conversion of 100V Inputs for Telecom/Automotive Supplies – Design Note 398

Greg Dittmer

Introduction

Automotive, telecom and industrial systems have harsh, unforgiving environments that demand robust electronic systems. In telecom systems the input rail can vary from 36V to 72V, with transients as high as 100V. In automotive systems the DC battery voltage may be 12V, 24V or 42V with load dump conditions causing transients up to 60V or more. The LTC®3810 is a current mode synchronous switching regulator controller that can directly step down input voltages up to 100V, making it ideal for these harsh environments. The ability to step down the high input voltage directly allows a simple single inductor topology, resulting in a compact high performance power supply—in contrast to the low side drive topologies that require bulky, expensive transformers.

Feature-Rich Controller

The LTC3810 drives two external N-channel MOSFETs using a synchronizable constant on-time, valley current mode architecture. A high bandwidth error amplifier provides fast line and load transient response. Strong 1Ω gate drivers minimize switching losses—often the dominant loss component in high voltage supplies—even when multiple MOSFETs are used for high current applications. The LTC3810 includes an internal linear regulator controller to generate a 10V IC/driver supply from the high voltage input supply with a single external SOT23 MOSFET. When the output voltage is above 6.7V, the 10V supply can be generated from the output, instead of the

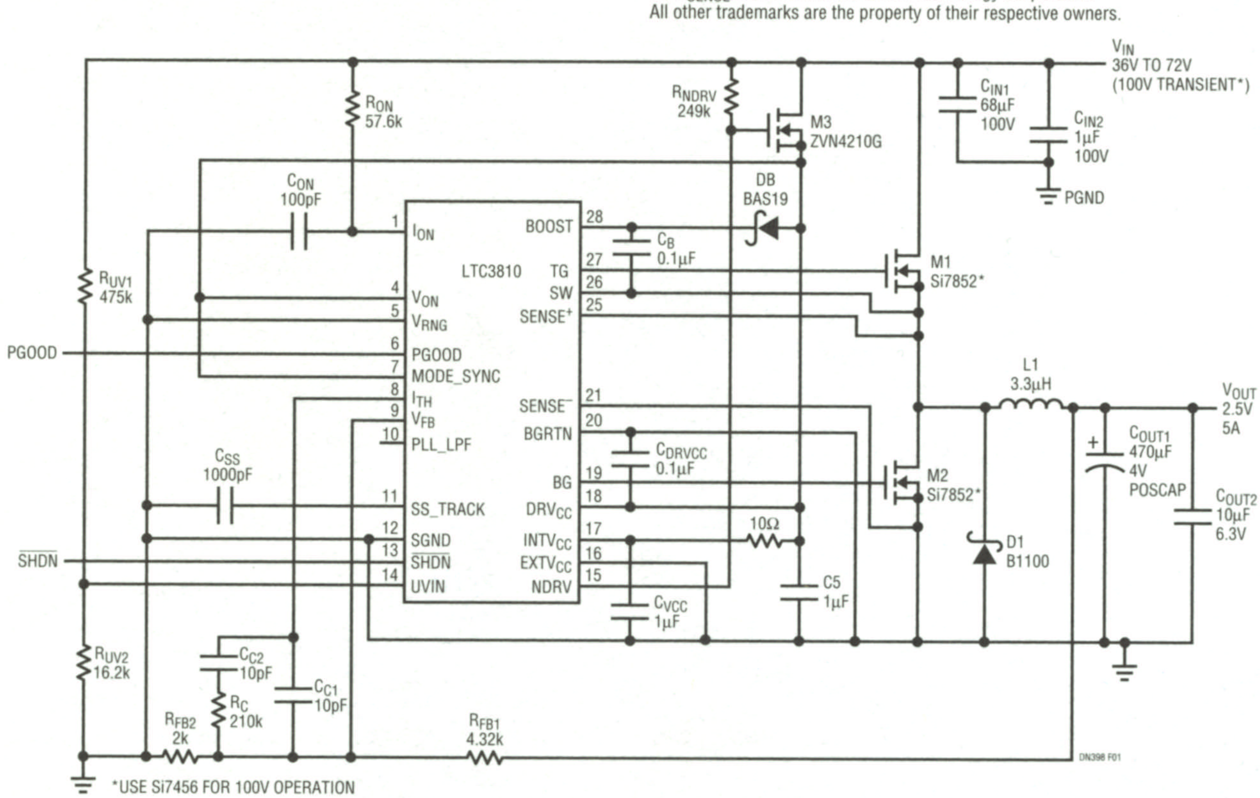

Figure 1. Compact 36V–72V to 2.5V/6A Synchronous Step-Down Converter

input, for higher efficiency. Other features include:

- Programmable cycle-by-cycle current limit, with tight tolerances, provides control of the inductor current during a short-circuit condition. No R_{SENSE}™ current sensing utilizes the voltage drop across the synchronous MOSFET to eliminate the need for a current sense resistor.
- Low minimum on-time (<100ns) for low duty cycle applications. The on-time is programmable with an external resistor and is compensated for changes in input voltage to keep switching frequency relatively constant over a wide input supply range.
- Precise 0.8V, ±0.5% reference over the operating temperature range of 0°C to 85°C.
- Phase-locked loop for external clock synchronization, selectable pulse-skip mode operation, tracking, programmable undervoltage lockout and power good output voltage monitor.
- 28-pin SSOP package with high voltage pin spacing.

High Efficiency 36V–72V to 2.5V/6A Power Supply

The circuit shown in Figure 1 provides direct step-down conversion of a typical 48V telecom input rail to 2.5V at 5A. With the 100V maximum DC rating of the LTC3810 and 80V for the MOSFETs, the circuit can handle input voltages of up to 80V without requiring protection devices (up to 100V if appropriate MOSFETs are used). This circuit demonstrates how the low minimum on-time of the LTC3810 enables high step-down ratio applications: 2.5V output from a 72V input at 250kHz is a 140ns on-time.

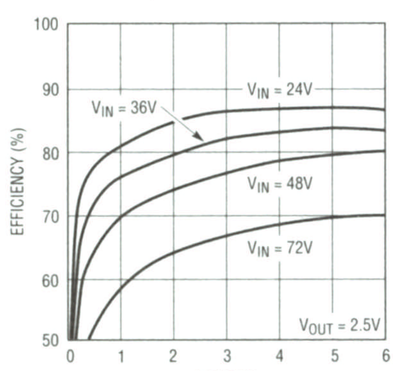

Figure 2. Efficiency of the Circuit in Figure 1

The frequency is set to 250kHz with the R_{ON} resistor to optimize efficiency while minimizing output ripple. Figure 2 shows mid-range efficiencies of 80% to 84% at 36V input and 65% to 70% at 72V input. Type II compensation is used to set the loop bandwidth to about 75kHz, which provides a 20µs response time to load transients (see Figure 3).

The V_{RNG} pin is set to 0V to set the current limit to about 8A (3A after foldback) during a short-circuit condition (see Figure 4). The resistor divider (R_{UV1}, R_{UV2}) sets the input supply undervoltage lockout to 24V, keeping the LTC3810 shut-down until the V_{IN} > 24V.

The LTC3810's internal linear regulator controller generates the 10V IC/driver supply ($INTV_{CC}$, DRV_{CC} pins) from the input supply with a single external MOSFET, M3. For continuous operation the power rating of M3 must be at least (72V – 10V) • (0.02A) = 1.2W. If another low voltage supply (between 6.2V and 14V) capable of supplying the ~20mA IC/driver current is available, this supply could be connected to $INTV_{CC}$/DRV_{CC} pins to increase efficiency by up to 10% at loads above 1A.

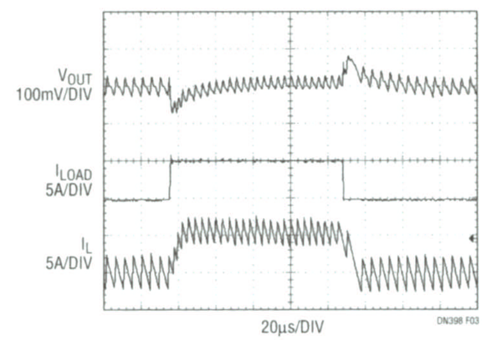

Figure 3. Load Transient Performance of Figure 1 Circuit Shows 20µs Response Time to a 5A Load Step

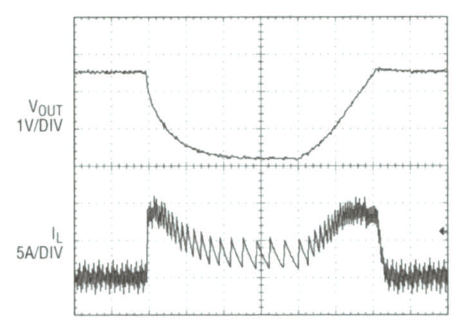

Figure 4. Short-Circuit Condition in Figure 1 Circuit Shows Tight Control of Inductor Current and Foldback

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on, MOSFET Q_4 switches off, and the load becomes effectively isolated from the dangerous transient.

The circuit now remains in its tripped state until reset. Under these conditions, Q_3 clamps Q_4's gate-source voltage to roughly 0V, thereby protecting the MOSFET itself from excessive gate-source voltages. Ignoring the negligibly small voltage across R_5, you can see that the reference voltage is $V_S \times R_4/(R_3+R_4)$ in volts. Because D_2's output turns on when the reference voltage exceeds 2.5V, you can rearrange the equation as $R_3=[(V_{ST}/2.5)-1]\times R_4$ in ohms, where V_{ST} is the required supply-voltage trip level. For example, if R_4 has a value of 10 kΩ, a trip voltage of 18V would require R_3 to have a value of 62 kΩ. When choosing values for R_3 and R_4 to set the desired trip voltage, ensure that they are large enough that the potential divider will not excessively load the supply. Similarly, avoid values that could result in errors due to the reference-input current.

When you first apply power to the circuit, you'll find that capacitive, bulb-filament, motor, and similar loads having large inrush current can trip the circuit breaker, even though their normal, steady-state operating current is below the trip level that R_6 sets. One way to eliminate this problem is to add capacitor C_2, which slows the rate of change of the voltage at the reference input. However, although simple, this approach has a serious disadvantage in that it slows the circuit's response time to a genuine overcurrent-fault condition.

Components C_1, R_1, R_2, and Q_1 provide an alternative solution. On power-up, C_1 initially discharges, causing Q_1 to turn on, thereby clamping the reference input to 0V and preventing the inrush current from tripping the circuit. C_1 then charges through R_1 and R_2 until Q_1 eventually turns off, releasing the clamp at the reference input and allowing the circuit to respond rapidly to overcurrent transients. With the values of C_1, R_1, and R_2, the circuit allows approximately 400 msec for the inrush current to subside. Selecting other values allows the circuit to accommodate any duration of inrush current you apply to a load. Once you trip the circuit breaker, you can reset it either by cycling the power or by pressing S_1, the reset switch, which connects across C_1. If your application requires no inrush protection, simply omit C_1, R_1, R_2, and Q_1 and connect S_1 between the reference input and 0V.

When choosing components, make sure that all parts are properly rated for the voltage and current levels they will encounter. The bipolar transistors have no special requirements, although these transistors, especially Q_2 and Q_3, should have high current gain, Q_4 should have low on-resistance, and Q_4's maximum drain-to-source and gate-to-source voltages must be commensurate with the maximum value of supply voltage. You can use almost any small-signal diode for D_1. As a precaution, it may be necessary to fit zener diodes D_3 and D_4 to protect D_2 if extremely large transient voltages are likely.

Although this circuit uses the 431 device, which is widely available from different manufacturers, for D_2, not all of these parts behave in exactly the same way. For example, tests on a Texas Instruments (www.ti.com) TL431CLP and a Zetex (www.zetex.com) ZR431CL reveal that the cathode current is 0A for both devices when the reference voltage is 0V. However, gradually increasing the reference voltage from 2.2 to 2.45V produces a change in cathode current ranging from 220 to 380 μA for the TL431CLP and 23 to 28 μA for the ZR431CL—roughly a factor of 10 difference between the two devices. You must take this difference in the magnitude of the cathode current into account when selecting values for R_7 and R_8.

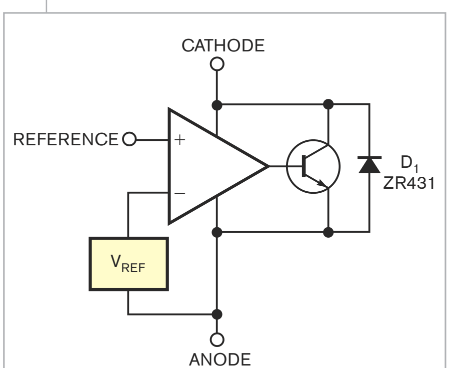

Figure 2 In this simplified view of the ZR431, the voltage at its reference input is compared with the internal voltage reference, which is nominally 2.5V.

The type of device you use for D_2 and the values you select for R_7 and R_8 can also have an effect on response time. A test circuit with a TL431CLP, in which R_7 is 1 kΩ and R_8 is 4.7 kΩ, responds within 550 nsec to an overcurrent transient. Replacing the TL431CLP with a ZR431CL results in a response time of approximately 1 μsec. Increasing R_7 and R_8 by an order of magnitude to 10 and 47 kΩ, respectively, produces a response time of 2.8 μsec. Note that the relatively large cathode current of the TL431CLP requires correspondingly small values of R_7 and R_8.

To set the overvoltage-trip level at 18V, R_3 and R_4 must have values of 62 and 10 kΩ, respectively. The test circuit then produces the following results: Using a TL431CLP for D_2, the circuit trips at 17.94V, and, using a ZR-431CL for D_2, the trip level is 18.01V. Depending on Q_2's base-emitter voltage, the overcurrent-detection mechanism is less precise than the overvoltage function. However, the overcurrent-detection accuracy greatly improves by replacing R_6 and Q_2 with a high-side current-sense amplifier that generates a ground-referred current proportional to load current. These devices are available from Linear Technology (www.linear.com), Maxim (www.maxim-ic.com), Texas Instruments, Zetex, and others.

The circuit breaker should prove useful in applications such as automotive systems that require overcurrent detection to protect against faulty loads and that also need overvoltage protection to shield sensitive circuitry from high-energy-load-dump transients. Other than the small current flowing in R_3 and R_4 and the current in D_2's cathode, the circuit draws no current from the supply in its normal, untripped state. EDN

Paralleling decreases autozero-amplifier noise by a factor of two

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Autozero amplifiers have almost zero drift and input-offset values of 1 to 20 μV. You can compensate for the initial voltage offset of an autozero amp in sensitive circuits, such as dc amplifiers and integrators, requiring the processing of voltages of 10 μV to 1 mV. Total compensation down to an offset of 0V, however, is an illusion because residual low-frequency output noise is still present in any autozero amp.

The Analog Devices (www.analog.com) AD8628 autozero amp has a low-frequency-noise value of 0.5 μV p-p at 0.1 to 10 Hz. If your application requires zero drift and low output noise, you can use the circuit in **Figure 1**. A quad autozero amp develops a gain of almost 1000. The resistor network comprising the R_3 resistors averages the output signals of these amplifiers to create the final output voltage.

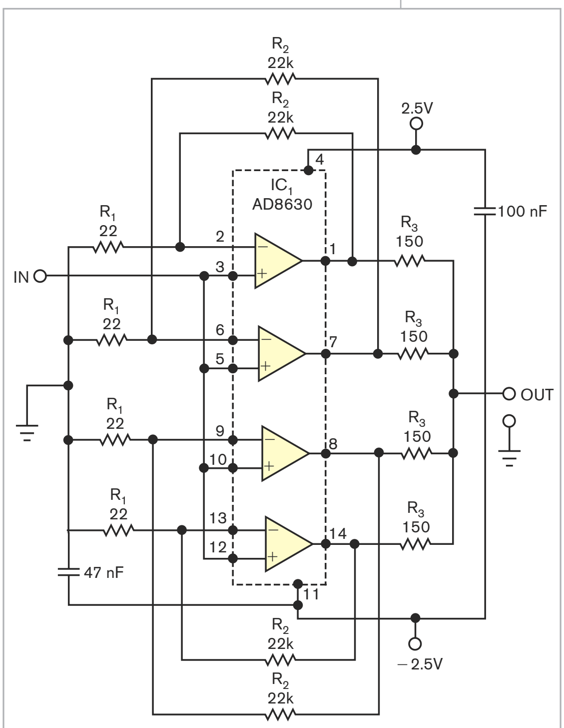

Figure 1 Use this circuit when your application requires zero drift and low output noise.

The quad autozero amps are the four sections of IC_1, an Analog Devices AD8630 (**Reference 1**). Quad integrated resistors having one common lead can substitute for the four R_3 resistors. The R_1 and R_2 resistors should be high-quality, precision, film devices with 0.5% or less tolerance. The tolerance of the R_3 resistors should not exceed 1%. The basis for decreasing the circuit's noise at the output in comparison with a single amplifier of IC_1 is the principle of averaging the signals containing the same deterministic component of random noise. If you assume that the amplifiers of IC_1 represent independent or uncorrelated noise sources that obey the gaussian distribution, then the standard deviation of the average of noise outputs of these sections is:

$$\sigma_{AVE2} = \frac{\sqrt{\sigma_X^2 + \sigma_Y^2}}{2},$$

where σ_X and σ_Y are the standard deviations of noise signals at outputs of the single respective amplifiers. If $\sigma_X = \sigma_Y$—an assumption that you can make without hesitation because the op amps reside in one chip—then:

$$\sigma_{AVE2} = \frac{\sigma_X}{\sqrt{2}}.$$

If you average four amplifiers, you obtain:

$$\sigma_{AVE4} = \frac{\sigma_X}{2}.$$

If the value of output resistance of the circuit, which is about $R_3/4 \approx 38\Omega$, is too high for your application, place a voltage follower between the output terminal and the next stage. EDN

REFERENCE

1 "AD8630 Quad, Zero Drift, Single-Supply, Rail-to-Rail Operational Amplifier," Analog Devices Inc, www.analog.com/en/prod/0,2877,AD8630,00.html.

Two transistors form high-precision, ac-mains ZCD

Djessas Zoheir, Constantine, Algeria

Many applications that use 110V/230V-ac mains require a ZCD (zero-crossing-detection) circuit for the ac-line voltage, for example, to synchronize the switching of loads. One method of ZCD uses a high-value current-limiting resistor or a voltage-resistive divider to sense the ac voltage at the controller's I/O pin. However, depending on whether the I/O pin is in TTL or Schmitt-trigger mode, the ZCD has a delay that depends on the threshold swing of the I/O pin and the slew rate of the power line. For example, assume a 230V, 50-Hz ac system voltage and a voltage divider of 100—that is, 230V/100=2.3V. Further, assume that the I/O pin triggers at 1V. This trigger level implies 1V×100=100V referenced to the 230V-ac mains. Thus, 100=230×sin(2×π×50×t) yields a delay of 1.43 msec, which represents 14.3% of the half-cycle period—a significant error.

Figure 1 shows a low-cost, efficient ZCD using two standard transistors. Coming directly from the ac mains,

the supply network comprising C_1, C_2, D_1, D_2, and R_1 forms a simple half-wave rectifier, which powers the ZCD. Q_1 toggles with the ac-mains-voltage ZCD. To compensate for the base-emitter gap, Q_2 acts as a diode to block the ac-positive cycle. For efficiency, the detector must sense the ac-mains cycles at as high a voltage as possible. This requirement drives the choice of the transistor. Q_2 and Q_1, low-noise, small-signal BC549B transistors, have collector-to-emitter-voltage limits of 30V. With this choice, you must attenuate the ac-mains voltage from 230 to 30V. (For a BC546 transistor, you can attenuate 230 to 80V.) Thus, the voltage-divider ratio is 30V/230V=13.4%, and the values of the divider resistors are $R_2/(R_3+R_2)=13.4/100$, or $R_3=6.46\times R_2$. R_2 and R_3 must be high enough for current limiting. The normalized value of R_3, 820 kΩ, means that R_2 is 820 kΩ/6.46=126.9 kΩ or 120 kΩ, the nearest standard-value resistor. With these values, Q_2 can block $230V\times R_2/(R_2+R_3)=29.3V$, which is less than the transistor's maximum rating of 30V.

Upon the ac-positive cycle, the base of Q_1 rises to approximately 0.6V through R_4. Q_2 acts as a simple diode. So, when the cycle voltage is higher than 0V, Q_2 is reverse-biased and blocks any current flow. At 0V, Q_2 is forward-biased, but it maintains 0.6V across the base-emitter junction, V_{BE}. Thus, the collector, or base, of Q_2, which connects to the base of Q_1, stays at 0.6V. Q_1 is saturated for the positive cycle, and the output voltage is low. At the ac's negative cycle, when the ac voltage is less than 0V, current flows through Q_2. Consequently, the base of Q_1, which connects to Q_2's collector, falls to less than 0.6V, which leads to the blocking of Q_1 and the output voltage's becoming high. Note that the base of Q_1 can reach about −30V from Q_2; you can add clamp diode D_3 for Q_1 junction protection higher than −1V. EDN

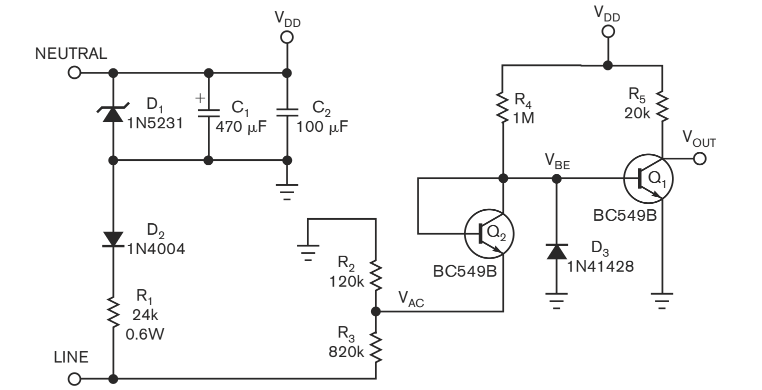

Figure 1 This simple two-transistor circuit accurately detects the zero crossing of the input ac mains.


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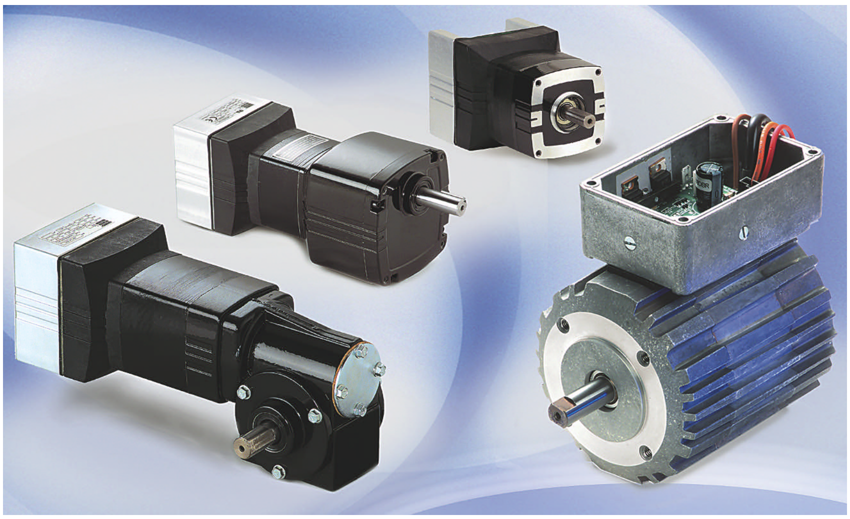
MOTION



Digital-PWM-controlled motion-control system integrates brushless-dc motor

Combining a control, a 24V-dc brushless motor, a gearhead, and an optical encoder allows the digital-PWM (pulse-width-modulation)-controlled version of the vendor's Integramotor to reduce wiring problems, assembly time, and EMI. The vendor's controls in type 22B/FV or 34B/FV Integramotors accept PWM input from an external motion controller or PLC (programmable-logic controller). Features include amplifier enable; direction input; dynamic braking; and a built-in 256-pulse/revolution, two-channel encoder. The digital-PWM Integramotor costs \$400 to \$600.

Bodine Electric Co, **www.bodine-electric.com**

Cable line suits one, two, or three axes of servo motion

Targeting motion applications, these cables are flat and encapsulated in glass-clear silicone. Available in one, two, or three axes of servo motion, each configuration provides options for 1000, 2000, and 3000W servomotors. The cables feature four shielded power cables and eight signal cables for each axis of motion. The silicone encapsulation provides a one-piece construction, creating a durable package. Additional features include a 1.5-in. bend radius; a 10 million-cycle lifetime before deforming, breaking, or wearing; and a −65 to +260°C temperature range. Impervious to water, steam, and chemicals, the Motion Series cables cost \$9 per foot for the 1000W model and \$20 per foot for the 3000W, one-axis cable.

Cicoil, www.cicoil.com

Incremental encoder provides more than 160,000 counts

The L15 incremental encoder allows 40,640 cycles per turn in control systems, allowing a 162,560 maximum count using the quadrature-detection option. The vendor claims that the internal electric multiplication boosts output resolutions 16 times with no degradation over overall encoder accuracy. Additional features include a servo-mount package, a 0.25-in.-diameter stainless-steel shaft, and the ability to accommodate a 5-lb radial or axial load. Measuring 1.5 in. in diameter, the L15 incremental encoder costs \$500.

BEI Industrial Encoders, www.beiied.com

Brushless-dc motor uses internal Hall-sensor feedback

The Pittman Elcom ST Series N2300 slotted, brushless-dc motor uses internal Hall-sensor feedback for linear-speed-torque characteristics, high starting torque, and variable-speed control. Measuring 2.3 in. in diameter, the motors come in 0.5-, 1-, 1.5-, and 2-in. stack lengths and provide high-energy neodymium-iron-boron magnets. Able to reach speeds as high as 8000 rpm, the motors also provide 40 oz-in. continuous torque. The Elcom ST Series N2300 costs \$58.

Ametek Technical & Industrial Products, www.ametektechnicalproducts.com

Mixed-signal chip targets motion and power-supply parts

Aiming at motion and power-supply parts in printer applications, the SABRe (structured architecture of bridges and regulators) mixed-signal chip features customizable motor drivers, regulators, ADCs, operational amplifiers, and voltage comparators. Some architectural changes are customizable using the serial interface or general-purpose I/Os; more complex functions are customizable with metal layers implementing macro functions. Functioning as the

productroundup

MOTION

master, the device manages the power section of the application with programmable PowerUp routines before the digital IC switches on. The device comprises four configurable bridges also functioning as switching regulators or power charges; a variable-voltage buck-switching regulator; a switching-regulator controller; a linear regulator; a multichannel, configurable, 9-bit ADC; two operational amplifiers; a bidirectional serial interface; and several general-purpose I/Os. Prices for the SABRe IC range from $2.20 to $2.50, depending on quantities.

STMicroelectronics, www.st.com

Linear actuator provides for mounting on 28-mm centers

Allowing mounting on 28-mm centers for multiactuator capabilities, the Model STA11 ServoTube linear actuator features a built-in solid-state position sensor and provides ±12 microns of repeatability and a 1V p-p sin/cos output. The device features a 92N peak force, a 4.7m/sec velocity, and the ability to accelerate instrumentation-type loads to as much as 25g. Additional features include an 11-mm thrust-rod diameter, a 26×61-mm forcer, and 75V actuator operation. The actuator also has a 14- to 232-mm stroke. The Model STA11 costs $793.

Copley Controls, www.copleycontrols.com

TEST AND MEASUREMENT

Cellular-field-measurement and network device features IDEN capability

The ZK-Sam cellular-field-measurement and networking-product line now includes IDEN (integrated digital enhanced network), which allows devices to analyze and compare IDEN and CDMA (code-division-multiple-access) networks using the same drive-test tools. The devices use a technology that requires no laptop to log the captured drive-test data. Not including phones or handsets, a single-technology ZK-Sam device costs $8000.

ZK Celltest, www.zk.com

USB 2.0 JTAG controller features SPI and I²C interface

Providing test vectors at a 100-MHz sustained test-clock frequency, the USB 2.0-based USB-1149.1/4E boundary-scan-test and in-system-programming controller features board testing and in-system programming of CPLDs, FPGAs, and flash memories at full theoretical programming speed. Direct I²C- and SPI (serial-peripheral-interface)-based device-programming capabilities provide boundary-scan-controller tests on the board and perform direct programming of serial EEPROM and flash memory without removing the JTAG connector or switching to a dedicated SPI or I²C programmer. Additional features include automatic signal-delay compensation for long cable runs to the unit under test, slew-rate control, an adjustable input threshold, a software-controllable signal-pin reassignment, and eight analog channels for measuring target supply voltages or other 5V-dc signals. The USB-1149.1/4E comes with cables, built-in self-test software, and plug-and-play Windows 2000/XP device drivers; it costs $4900.

Corelis, www.corelis.com

Extender board provides access to both sides of test boards

Suiting use with payload or node slots, the VXS payload-extender boards remove a circuit card from a card cage or enclosure, providing access to both sides of the test board for testing or debugging. The device features test points on each line of the 160-pin connector and the MultiGig P0 connector. The VXS payload-extender boards cost $3000.

Elma Bustronics, www.bustronic.com

Signal-conditioning system features personality modules

The DaqScribe DSC-2200 series of signal-conditioning systems and the DSC-2200.Net network-centric data-acquisition system come in 2U rack-mount enclosures. DSC-2200 supports 32 channels of signal conditioning that are individually programmable to its own personality module per chassis. Personality modules include the DSC-2210 for programmable amplifications and filtering and the DSC-2220 for strain-gauge conditioning. The device can select 0.1 to 1000 user-programmable-gain settings and four-pole Bessel-, Butterworth-, or Chebyshev-filter settings with three lowpass selections in addition to a wide-band option per channel. Supporting 1-MHz-per-channel analog bandwidth, the systems provide Ethernet connec-

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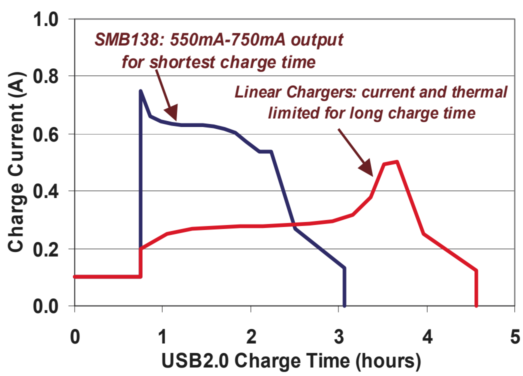
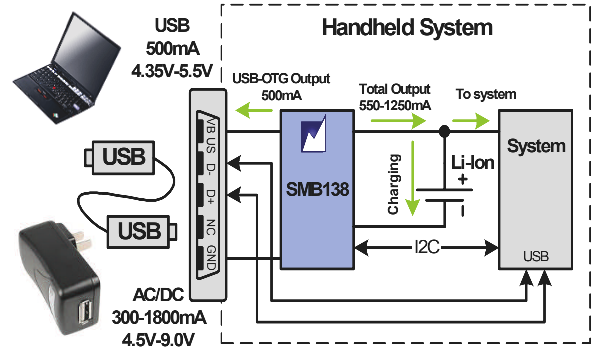


Single Mini/Micro-USB Interface for Data/Power Enables Ultra-Thin Applications

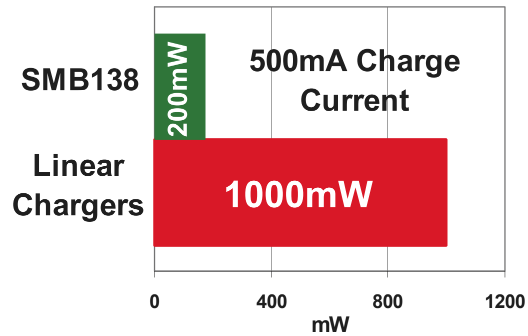


Built-In USB On-the-Go (OTG) Support up to 500mA

SMB138 Features

- TurboCharge™* for 50% Current Gain - Up to 1250mA
- USB On-the-Go (OTG) Power Support (+5V @ 500mA)
- +3.5V to +9.1V Operating Input (+16V Protection Built-In)
- 3MHz Switch-Mode Operation (Chip Inductors)
- I²C Programmable (Volatile and Non Volatile)
  - Fast/Pre-Charge/Termination Current
  - Pre-Charge/Float Voltage Thresholds
  - Battery Temp/Safety Watchdog Timers
- Built-in Safety
  - Input OV Protection to +16V
  - Battery OV/OC Protection
  - Trickle Charge for Deeply-Discharged Cells
  - Safety timers/Digital Fault Monitors
- 2mm x 3mm CSP Packaging

Switch-Mode Operation Cuts Power Loss and Dissipation by 80% vs. Linear Chargers



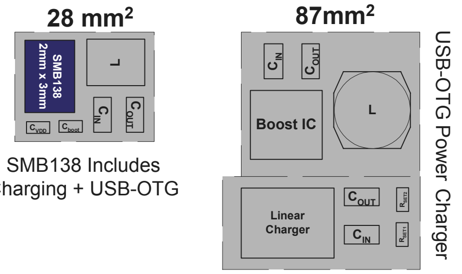
SMB138 Applications

- Mobile/Smart Phones
- Digital Cameras/Camcorders
- Portable Media Players/Games
- Handheld GPS Terminals

Chip-Scale Package, High Integration and Tiny Inductor Uses 66% less PCB Area

SMB138
28 mm²

Competitor
87mm²



SMB138 Includes Charging + USB-OTG

*Patent pending

TEST AND MEASUREMENT

tivity using GUI-based software. Supporting low-speed to midspeed network-centric applications, the DSC-2200.Net uses a 16-bit, 1-MHz ADC with an Ethernet controller to the DSC-2200. The LXI-compliant .Net system supports 16 to 256 channels of analog input through a master unit, allowing you to synchronize multiple units for higher channel counts, and provides user-programmable sampling at bandwidths as high as 1 MHz at 16-bit resolution. The DSC-2210, DSC-2220, and DSC-2240 cost $9995, $14,995, and $11,995, respectively; the DSC-2200.Net costs $2500 more.

GE Fanuc Embedded Systems, **www.gefanucembedded.com**

Hub option allows synchronization of 270 cards

The System Star Hub option for the UltraFast oscilloscope/digitizer, AWG (arbitrary-waveform generator), and digital-I/O and digital-pattern-generator PCI card allows the installation and synchronization of 270 cards in multiple computers. This feature enables the development of systems with 4336 analog channels or 8672 digital channels. The option requires the System Star Hub Master option for the first computer, and additional computers require System Star Hub Slaves. The Star Hub option costs $490 for five-card synchronization and $990 for 16-card synchronization. The System Star Hub Master costs $2800; the System Star Hub Slaves cost $590 for as many as five cards and $990 for as many as 16 cards.

Strategic Test, **www.strategic-test.com**

MICROPROCESSORS

IP-communication-controller chip functions as a coprocessor and router

Working as a coprocessor offloading IP (Internet Protocol) and network-security protocols from the host processor, the iChipSec CO2128 secure-IP-communication-controller chip also acts as a router, access point, or gateway for LAN, Wi-Fi, and modem platforms. The device provides a 10/100BaseT Ethernet MAC (media-access controller), a USB 2.0 full-speed host and device, a high-speed parallel bus, an external bus, an SPI (serial-peripheral interface), a two-wire interface, and USART interfaces. Security features include a random-number generator, an SHA (secure-hash-algorithm)-1/256 accelerator, an AES (Advanced Encryption Standard)-128/192/256 accelerator, 3DES (Triple Data Encryption Standard), SSL3 (Secure Socket Layer 3)/TLS1 (Transport Layer Security 1), and WEP (Wired Equivalent Privacy)/WPA2 (Wi-Fi Protected Access) encryption for Wi-Fi. The device uses an ARM7 core processor, a real-time operating system, and a security- and networking-protocol stack. A parallel interface provides 32-Mbps support with UDP (User Datagram Protocol)/IP hardware acceleration. The hardware also accelerates data encryption/decryption. The vendor's AT+i Protocol high-level API functions as the logical interface between the host application and the chip. The CO2128 costs $6; the II-EVB-630 evaluation board for secure Wi-Fi, LAN, cellular, or dial-up access costs $1725.

Connect One, **www.connectone.com**

BSP provides for simulations of Diamond Standard processors

The BSP (board-support package) supports Avnet LX60 FPGA boards targeting high-speed hardware-based simulations of the Diamond Standard processor family. The Diamond Standard SDK (software-development kit) comprises the Xtensa Xplorer IDE (integrated development environment), a code-development tool chain, and an ISS (instruction-set simulator) and is compatible with the Avnet LX60 boards. The device uses a feedback compilation, and the Xtensa C/C++ compiler uses these statistics and recompiles the program to increase speed by placing frequent branches in straight-line code. It compiles less frequently executed routines for code size rather than speed. This feature provides a 5 to 15% speed increase and a 15% reduction in code size. The device also features an Ethernet interface on the Avnet LX60. The BSP supporting Diamond Standard 108 Mini, Diamond Standard 212GP, Diamond Standard 232L, and Diamond Standard 570T processors costs $3000 and suits use on an unlimited number of Avnet LX60 boards.

Tensilica, **www.tensilica.com**

Document-imaging SOC features SoftFax and SmartDAA technology

Targeting use in Panasonic's facsimile machines, the CX95410 document-imaging SOC (system on chip) includes the vendor's SoftFax technology and SmartDAA technology. Features include a 180-MHz, 32-bit RISC processor; a 120-MHz DSP-based image processor; and three 288-MHz, flexible-I/O processors. The SOC also provides an optional software-based voice-compression/decompression feature. The CX95410 is available in a 16-pin LQFP and sells for $5 to $10.

Conexant Systems, **www.conexant.com**

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LOOKING AHEAD

TO SEMICON WEST

Arguably the original conference concerning semiconductor manufacturing, SEMIcon West, the SEMI (Semiconductor Equipment and Materials International) organization's annual West Coast conference, runs July 16 through 20 at San Francisco's Moscone Center. The event is far too large and diverse to summarize in a paragraph, but it spans topics from business management for semiconductor manufacturers to technical sessions on process technology and equipment. Keynotes this year will reflect two important new themes that are rippling through the semiconductor industry: the growing integration of design with manufacturing and the growing influence of the energy industry in the semiconductor world. Two cases in point: In a Wednesday-afternoon keynote, Rhone Resch, president of the Solar Energy Industries Association, will argue that solar energy constitutes the next great opportunity for the semiconductor industry. And Thursday, Aart de Geus, chairman and chief executive officer of Synopsys, whom you might expect to hear at DAC (Design Automation Conference) rather than at SEMIcon, will offer a keynote on bridging design and manufacturing.

LOOKING BACK

AT REALLY DENSE AUDIO RECORDING

A small magnetic sound head provides lip-movement synchronization between 8-mm movie films and their soundtracks. A special amplifier enables the head to perform both recording and pickup functions. Designed by Telefunken GmbH, the tiny sound head's pole shoe is only 0.02 inches thick, with an air gap 0.0002 inches in width. The head works with a magnetic soundtrack 1⁄32 of an inch wide, which the film manufacturer must deposit alongside the perforations in the 8-mm movie film. At 24 frames per second, the quality of reproduction compares favorably with that of a good tape recorder, according to the manufacturer.

—*Electrical Design News*, June 1957

LOOKING AROUND

AT THE STATE OF IC DESIGN

This week, much of the attention of the chip-design profession focuses on the Design Automation Conference in San Diego. For many, the sight will be worrying: remarkably few new ideas or even really new tools. One possible explanation is that chip design has run up against a technical/economic ceiling and that fewer and fewer design teams, often using their own tools, will keep up the climb to more and more challenging geometries. But there is an alternative view as well: that this is not a ceiling but a landing—a symptom that process technology has outrun the ability of tools and design teams to exploit it. If this is the case—and history suggests it is more likely than the end-of-history scenario—then 2007 could be a pause before another burst of growth and creativity in chip design, waiting only for a few key insights to unleash the breakthrough. Time will tell, as usual, what forecasting can't.

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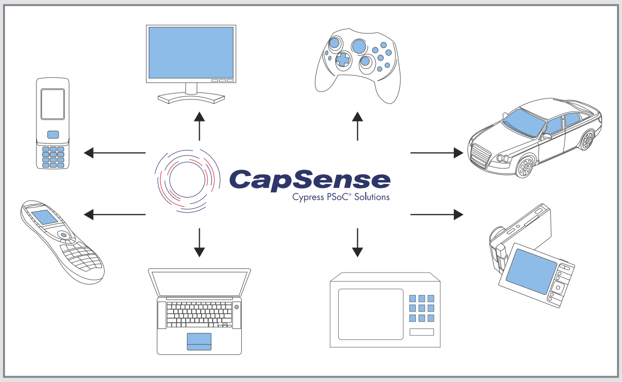

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